

# Signal Isolated RS-485 Transceiver With Integrated DC to DC Converter

Datasheet (EN) 1.0

## Product Overview

NSiP83086 series are high reliability isolated full duplex RS-485 transceiver with integrated DC to DC converter. The NSiP83086 isolated DC to DC converter uses on-chip transformer. The feedback PWM signal is sent to primary side(Isolator Side1) by a digital isolator based on Novosense capacity isolation technology. The NSiP83086 series are safety certified by UL1577 supporting 5kVrms insulation withstand voltage, while the high integrated solution can help to simplify system design and improve reliability.

The Bus pins of NSiP83086 are protected from  $\pm 8kV$  system level ESD to  $GND_2$ . The device features a fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The device have  $96k \Omega$  input impedance that allows up to 256 transceivers on the bus.

## Key Features

- Up to 5000Vrms Insulation voltage
- ISO-Power integrated isolated DC-to-DC converter
- I/O voltage range supports 1.8~5.5V MCU
- Power supply voltage:
  - VDD: 4.5V to 5.5V for NSiP83086
  - 3V to 5.5V for NSiP83086C and NSiP83086V
  - VDDL: 1.8V to 5.5V
- Over current and over temperature protection
- High CMTI:  $\pm 150kV/us$
- Data rate: 16Mbps
- Up to 256 transceivers on the bus
- High system level EMC performance:
  - BUS Pins meet IEC61000-4-2  $\pm 8kV$  ESD
  - Other Pins meet IEC61000-4-2  $\pm 7kV$  ESD
- Operation temperature:  $-40^{\circ}C \sim 105^{\circ}C$
- RoHS-compliant packages: SOW20 SOW16

## Safety Regulatory Approvals

- UL recognition: up to  $5000V_{RMS}$  for 1 minute per UL1577
- CQC certification per GB4943.1-2022
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

## Applications

- Industrial automation system
- Isolated RS-485 communication
- Smart electric meter and water meter
- Security and protection monitoring

## Device Information

Part Number	Package	Body Size
NSiP83086(C)(V)-DSWTR	SOW20	12.80mm × 7.50mm
NSiP83086(V)-DSWR	SOW16	10.30mm x 7.50mm

Note: (C), (V) could be empty representing 5V output version. V represents 3.3V output version, C version has SEL pin which can choose 3.3/5V output

## Functional Block Diagrams

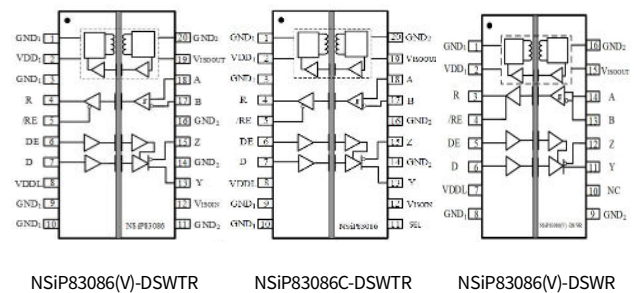


Figure 1. NSiP83086 Block Diagrams

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### 1. Pin Configuration and Functions

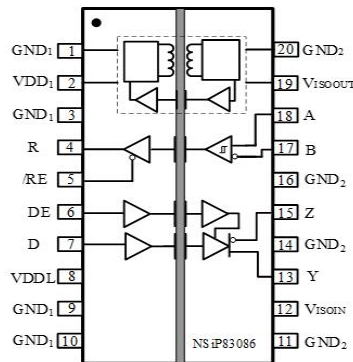


Figure 1.1 NSiP83086(V)-DSWTR Package

Table1.1 NSiP83086(V)-DSWTR Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
2	VDD <sub>1</sub>	Power Supply for Isolator Side 1 ,It is recommended this pin have a 0.1μF + 10 μF capacitor to GND <sub>1</sub> (Pin1,Pin3 )
3	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
4	R	Receiver output
5	/RE	Receiver enable input, this is an active low input
6	DE	Driver enable input, this is an active high input
7	D	Driver transmit data input
8	VDDL	I/O Power Supply input, Side1 I/O logic level
9	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
10	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
11	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
12	VISOIN	Isolated power supply input. This pin must be connected externally to VISOOUT. It is recommended this pin have a 0.1 μF capacitor to GND <sub>2</sub> (Pin11). Connect this pin to VISOOUT through a ferrite bead and short trace length for operation.
13	Y	Non-inverting Driver Output. When the driver is disabled, or when VDDL is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
14	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
15	Z	Inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
16	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
17	B	Inverting Receiver Input

18	A	Non-inverting Receiver Input
19	V <sub>ISOOUT</sub>	Isolated Power Supply Output. This pin must be connected externally to V <sub>ISOIN</sub> . It is recommended this pin have a 0.1 μF and 10μF capacitor to GND <sub>2</sub> (Pin20). Connect this pin through a ferrite bead and short trace length to V <sub>ISOIN</sub> for operation.
20	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2

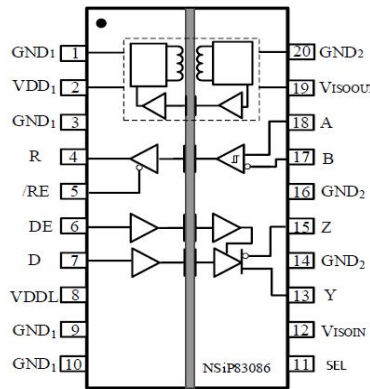


Figure 1.2 NSiP83086C-DSWTR Package

Table1.2NSiP83086C-DSWTR Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
2	VDD <sub>1</sub>	Power Supply for Isolator Side 1, It is recommended this pin have a 0.1μF + 10 μF capacitor to GND <sub>1</sub> (Pin1,Pin3 )
3	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
4	R	Receiver output
5	/RE	Receiver enable input, this is an active low input
6	DE	Driver enable input, this is an active high input
7	D	Driver transmit data input
8	VDDL	I/O Power Supply input, Side1 I/O logic level
9	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
10	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
11	SEL	VISO output voltage select, V <sub>ISOOUT</sub> =5V when SEL is floating or connect to V <sub>ISOIN</sub> , V <sub>ISOOUT</sub> =3.3V when SEL short to GND <sub>2</sub>
12	V <sub>ISOIN</sub>	Isolated power supply input. This pin must be connected externally to V <sub>ISOOUT</sub> . It is recommended this pin have a 0.1 μF capacitor to GND <sub>2</sub> . Connect this pin to V <sub>ISOOUT</sub> through a ferrite bead and short trace length for operation.
13	Y	Non-inverting Driver Output. When the driver is disabled, or when VDDL is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
14	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2

15	Z	Inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
16	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
17	B	Inverting Receiver Input
18	A	Non-inverting Receiver Input
19	V <sub>ISOOUT</sub>	Isolated Power Supply Output. This pin must be connected externally to V <sub>ISOIN</sub> . It is recommended this pin have a 0.1 μF and 10μF capacitor to GND <sub>2</sub> (Pin20). Connect this pin through a ferrite bead and short trace length to V <sub>ISOIN</sub> for operation.
20	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2

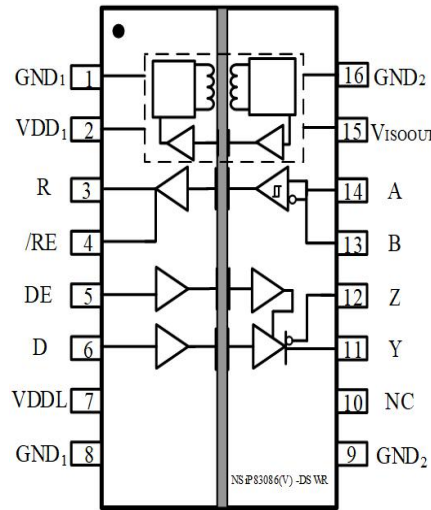


Figure 1.3 NSiP83086(V)-DSWR Package

Table1.3NSiP83086(V)-DSWR Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
2	VDD <sub>1</sub>	Power Supply for Isolator Side 1. It is recommended this pin have a 0.1 μF + 10 μF capacitor to GND <sub>1</sub> (Pin1)
3	R	Receiver output
4	/RE	Receiver enable input, this is an active low input
5	DE	Driver enable input, this is an active high input
6	D	Driver transmit data input
7	VDDL	I/O Power Supply input, Side1 I/O logic level
8	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
9	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
10	NC	Not Connected

11	Y	Non-inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
12	Z	Inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
13	B	Inverting Receiver Input
14	A	Non-inverting Receiver Input
15	V <sub>ISOOUT</sub>	Isolated Power Supply Output. It is recommended this pin have a 0.1 $\mu$ F and 10 $\mu$ F capacitor to GND <sub>2</sub> (Pin16).
16	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2.

## 2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD,VDDL	-0.5		6	V	
Maximum Input Voltage	/RE, DE, D	-0.4		VDDL+0.4	V	
Driver Output/Receiver Input Voltage	V <sub>A</sub> , V <sub>B</sub> , V <sub>Y</sub> , V <sub>Z</sub>	-7		12	V	
R output current	I <sub>o</sub>	-15		15	mA	
Operating Temperature	Topr	-40		105	°C	
Storage Temperature	Tstg	-40		150	°C	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

## 3. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
NSiP83086 Power Supply Voltage	VDD	4.5	5	5.5	V
NSiP83086C and NSiP83086V Power Supply Voltage	VDD	3	3.3/5	5.5	V
Operating Temperature	Topr	-40		105	°C
Side1 High Level Input Voltage	V <sub>IH</sub>	0.7*VDDL		VDDL	V
Side1 Low Level Input Voltage	V <sub>IL</sub>	0		0.3*VDDL	V
Data rate	DR			16	Mbps

## 4. Thermal Information

Parameters	Symbol	SOW20	SOW16	Unit
IC Junction-to-Air Thermal Resistance	θ <sub>JA</sub>	68.5	61	°C/W
Junction-to-top characterization parameter	ψ <sub>JT</sub>	17.1	10.2	°C/W
Junction-to-board characterization parameter	ψ <sub>JB</sub>	50.9	37.2	°C/W

## 5. Specifications

### 5.1. DC Electrical Characteristics

(VDD=4.5V~5.5V, VDDL=1.8~5.5V, Ta=-40 °C to 105 °C . Unless otherwise noted, Typical values are at VDD=VDDL=5V, V<sub>ISOOUT</sub>=5V, Ta = 25 °C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power supply voltage NSiP83086	VDD <sub>1</sub>	4.5		5.5	V	
	VDDL	1.8		5.5	V	
Power supply voltage NSiP83086C/NSiP83086V	VDD <sub>1</sub>	3		5.5	V	
	VDDL	1.8		5.5	V	
Supply current condition: VDD=4.5V~5.5V, VDDL=1.8~5.5V, Ta=-40 °C to 105 °C.						
Supply current V <sub>ISOOUT</sub> = 5V	IDD (500kbps)		72	90	mA	VDD=5V VDDL=3.3V R <sub>L</sub> =120 Ω
			118	140	mA	VDD=5V VDDL=3.3V R <sub>L</sub> =54 Ω
	IDD (16Mbps)		100	130	mA	VDD=5V VDDL=3.3V R <sub>L</sub> =120 Ω
			130	160	mA	VDD=5V VDDL=3.3V R <sub>L</sub> =54 Ω
IDD <sub>L</sub>			5	mA		
Supply current condition: VDD=3~5.5V, VDDL=1.8~5.5V, Ta=-40 °C to 105 °C.						
Supply current V <sub>ISOOUT</sub> = 3.3V	IDD (500kbps)		40	55	mA	VDD=5V VDDL=3.3V R <sub>L</sub> =120 Ω
			61	80	mA	VDD=5V VDDL=3.3V R <sub>L</sub> =54 Ω
	IDD (16Mbps)		45	65	mA	VDD=5V VDDL=3.3V R <sub>L</sub> =120 Ω
			60	80	mA	VDD=5V VDDL=3.3V R <sub>L</sub> =54 Ω
IDD <sub>L</sub>			5	mA		
Isolated supply voltage	V <sub>ISOOUT</sub>		5		V	NSiP83086
	V <sub>ISOOUT</sub>		3.3/5		V	NSiP83086C
	V <sub>ISOOUT</sub>		3.3		V	NSiP83086V
Thermal-Shutdown Threshold	T <sub>TS</sub>		165		°C	
Thermal-Shutdown Hysteresis	T <sub>TSH</sub>		15		°C	
Common Mode Transient Immunity	CMTI	100	150		kV/us	<a href="#">Figure 5.12</a>
<b>Side1</b>						
Input High Voltage	V <sub>IH</sub>	0.7*VDDL			V	DE, D, /RE
Input Low Voltage	V <sub>IL</sub>			0.3*VDDL	V	DE, D, /RE
Input Current	I <sub>I</sub>	-20		20	uA	D, DE, /RE



Output Voltage High	$V_{OH}$	$0.8 \cdot V_{DDL}$			V	$I_{OH} = -4\text{mA}$
Output Voltage Low	$V_{OL}$			$0.2 \cdot V_{DDL}$	V	$I_{OL} = 4\text{mA}$
Output Short-Circuit Current	$I_{OSR}$			150	mA	$0 \leq V_R \leq V_{DDL}$
Three-State Output Current	$I_{OZR}$			15	uA	$0 \leq V_R \leq V_{DDL}$ , /RE = high
Input Capacitance	$C_{IN}$		2		pF	DE, D, /RE
<b>Driver</b>						
Differential Output Voltage	$ V_{OD} $			5.5	V	No Load, $V_{ISOOUT}=5\text{V}$
		2.7		5.5	V	<a href="#">Figure 5.7</a> , $R_L=120\Omega$ , $V_{ISOOUT}=5\text{V}$
		2.1		5.5	V	<a href="#">Figure 5.7</a> , $R_L=54\Omega$ (RS-485), $V_{ISOOUT}=5\text{V}$
Change in magnitude of the differential output voltage	$\Delta V_{OD} $			0.2	V	, $R_L=120\Omega$ or $R_L=54\Omega$ , $V_{ISOOUT}=5\text{V}$
Common-Mode Output Voltage	$ V_{OC} $			3	V	, $R_L=120\Omega$ or $R_L=54\Omega$ , $V_{ISOOUT}=5\text{V}$
Change in Magnitude of Common-Mode Voltage	$\Delta V_{OC} $			0.2	V	, $R_L=120\Omega$ or $R_L=54\Omega$ , $V_{ISOOUT}=5\text{V}$
Driver Short-Circuit Output Current	$I_{OSD}$			200	mA	$0 \leq V_{Test} \leq 12\text{V}$
		-200			mA	$-7\text{V} \leq V_{Test} \leq 0\text{V}$
Output Leakage Current (Y and Z) Full-Duplex	$I_o$			200	uA	DE=0V, $V_{Test}=12\text{V}$
		-200			uA	DE=0V, $V_{Test}=-7\text{V}$
<b>Receiver</b>						
Input Current (A and B)	$I_A, I_B$			200	uA	DE=0V, $V_{ISOIN}=0\text{V}$ , $V_{Test}=12\text{V}$
		-200			uA	DE=0V, $V_{ISOIN}=0\text{V}$ , $V_{Test}=-7\text{V}$
Receiver Differential Threshold Voltage	$V_{TH}$	-200	-125	-10	mV	$V_{CM}=0\text{V}$
Receiver Input Hysteresis	$\Delta V_{TH}$		15		mV	$V_A+V_B=0$
Receiver Input Resistance	$R_{IN}$	96			k $\Omega$	$-7\text{V} \leq V_{CM} \leq 12\text{V}$ , DE=0V

### 5.2. Switching Electrical Characteristics

(VDD=3V~5.5V,VDDL=1.8~5.5V, Ta=-40°C to 105°C. Unless otherwise noted, Typical values are at VDD=VDDL = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
<b>Driver</b>						
Maximum Data Rate	f <sub>MAX</sub>			16	Mbps	
Driver Propagation Delay	t <sub>PLH</sub>		22	60	ns	See Figure 5.8, R <sub>L</sub> =54Ω, C <sub>L</sub> =50pF
	t <sub>PHL</sub>		21	60	ns	See Figure 5.8, R <sub>L</sub> =54Ω, C <sub>L</sub> =50pF
Driver Pulse Width Distortion,  t <sub>PHL</sub> - t <sub>PLH</sub>	t <sub>skew</sub>		1	8	ns	See Figure 5.8, R <sub>L</sub> =54Ω, C <sub>L</sub> =50pF
Driver Output Falling Time or Rising time	t <sub>F</sub>			15	ns	See Figure 5.8, R <sub>L</sub> =54Ω, C <sub>L</sub> =50pF
	t <sub>R</sub>			15	ns	See Figure 5.8, R <sub>L</sub> =54Ω, C <sub>L</sub> =50pF
Driver Enable to Output High	t <sub>ZH</sub>		22.8	50	ns	See Figure 5.9, R <sub>L</sub> =120Ω, C <sub>L</sub> =50pF
Driver Enable to Output Low	t <sub>ZL</sub>		19.1	50	ns	See Figure 5.9, R <sub>L</sub> =120Ω, C <sub>L</sub> =50pF
Driver Disable to Output High	t <sub>HZ</sub>		28	50	ns	See Figure 5.9, R <sub>L</sub> =120Ω, C <sub>L</sub> =50pF
Driver Disable to Output Low	t <sub>LZ</sub>		27.1	50	ns	See Figure 5.9, R <sub>L</sub> =120Ω, C <sub>L</sub> =50pF
<b>Receiver</b>						
Maximum Data Rate	f <sub>MAX</sub>	16			Mbps	
Receiver Propagation Delay	t <sub>PLH</sub>		65.8	140	ns	See Figure 5.10, C <sub>L</sub> =15pF
	t <sub>PHL</sub>		71.4	140	ns	See Figure 5.10, C <sub>L</sub> =15pF
Receiver Pulse Width Distortion,  t <sub>PHL</sub> - t <sub>PLH</sub>	t <sub>skew</sub>		5.6	12	ns	See Figure 5.10, C <sub>L</sub> =15pF
Receiver Output Falling Time or Rising time	t <sub>F</sub>			15	ns	See Figure 5.10, C <sub>L</sub> =15pF
	t <sub>R</sub>			15	ns	See Figure 5.10, C <sub>L</sub> =15pF
Receiver Enable to Output High	t <sub>ZH</sub>		6	15	ns	See Figure 5.11, R <sub>L</sub> =1kΩ, C <sub>L</sub> =15pF
Receiver Enable to Output Low	t <sub>ZL</sub>		6	15	ns	See Figure 5.11, R <sub>L</sub> =1kΩ, C <sub>L</sub> =15pF
Receiver Disable to Output High	t <sub>HZ</sub>		8	15	ns	See Figure 5.11,

						$R_L=1k\Omega, C_L=15pF$
Receiver Disable to Output Low	$t_{LZ}$	8	15	ns		See Figure 5.11, $R_L=1k\Omega, C_L=15pF$

### 5.3. Typical Performance Characteristics

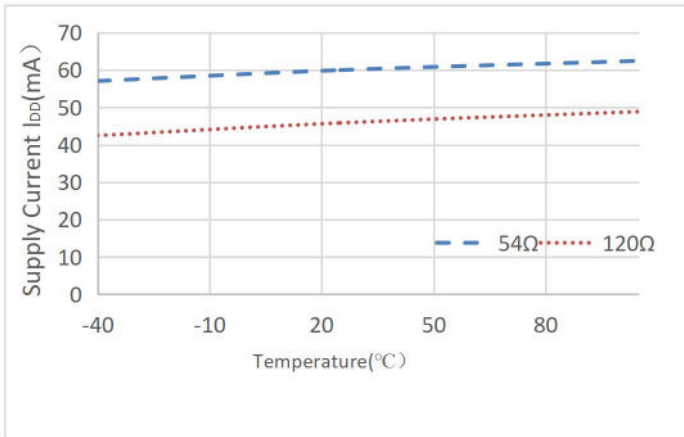


Figure 5.1 NSiP83086 supply current vs Temperature  
(Data Rate=16MHz, DE=VDDL, /RE=GND, VDD=5V, VISOOUT=3.3V)

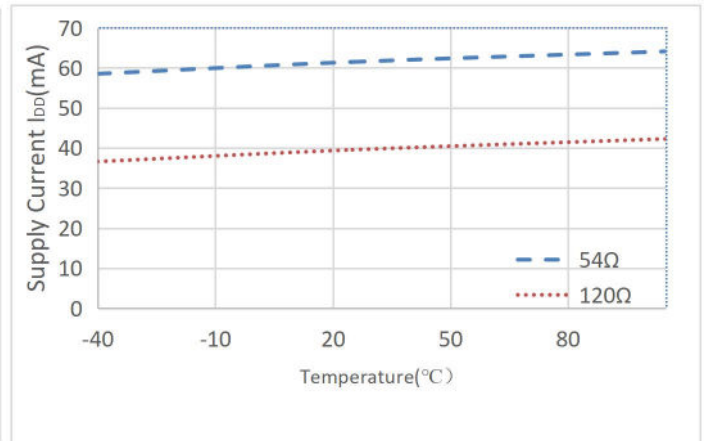


Figure 5.2 NSiP83086 supply current vs Temperature  
(Data Rate=500KHz, DE=VDDL, /RE=GND, VDD=5V, VISOOUT=3.3V)

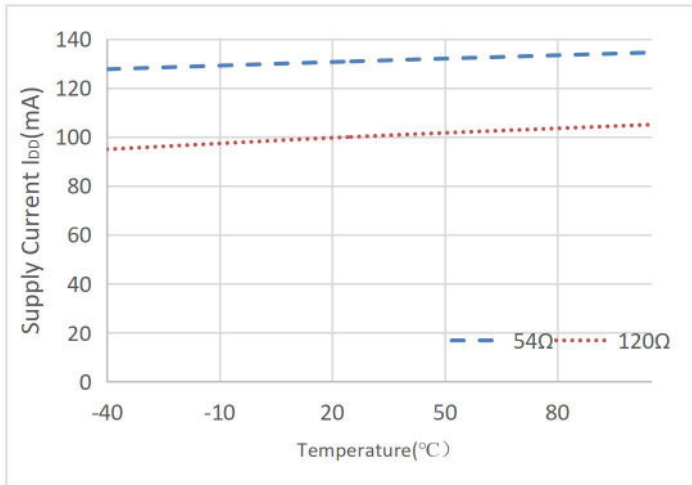


Figure 5.3 NSiP83086 supply current vs Temperature  
(Data Rate=16MHz, DE=VDDL, /RE=GND, VDD=5V, VISOOUT=5V)

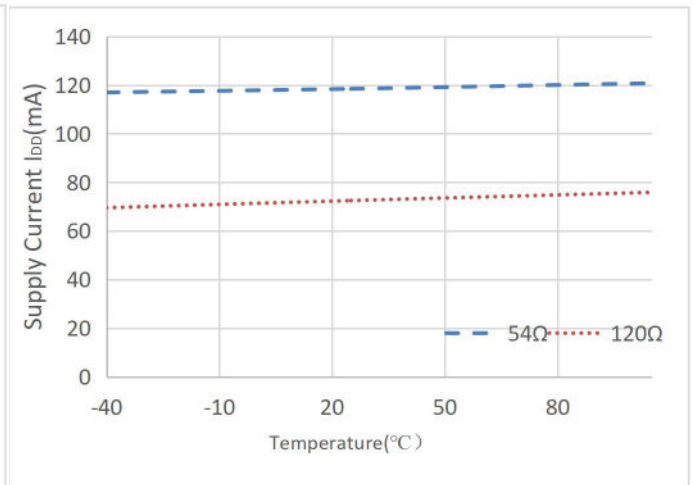


Figure 5.4 NSiP83086 supply current vs Temperature  
(Data Rate=500KHz, DE=VDDL, /RE=GND, VDD=5V, VISOOUT=5V)

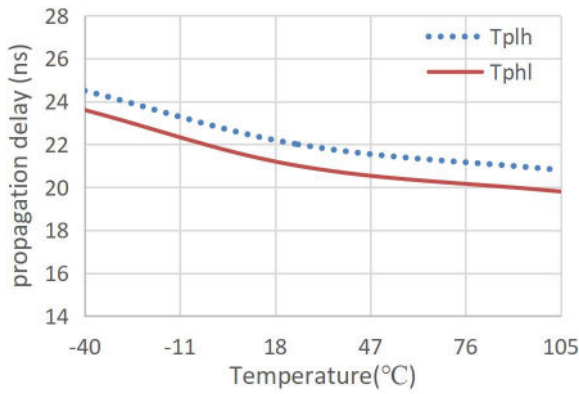


Figure 5.5 Driver Propagation Delay vs Temperature

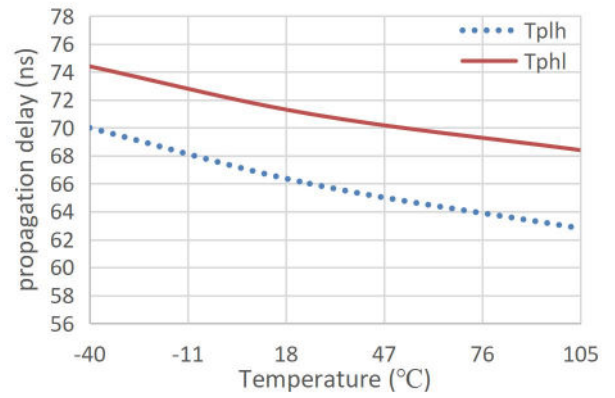


Figure 5.6 Receiver Propagation Delay vs Temperature

### 5.4. Parameter Measurement Information

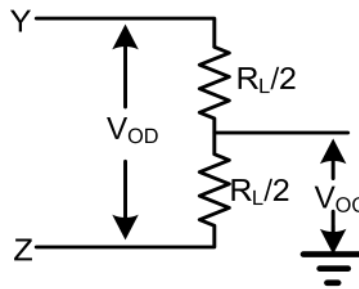


Figure 5.7 Driver DC Test Load

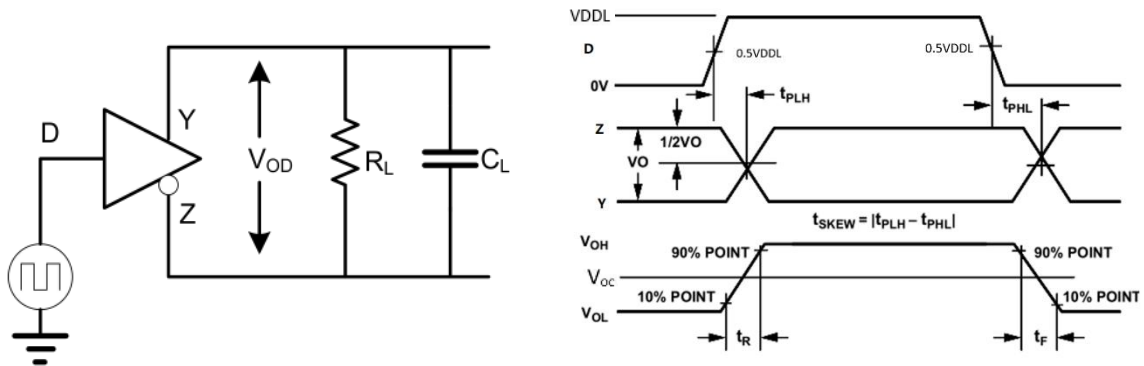
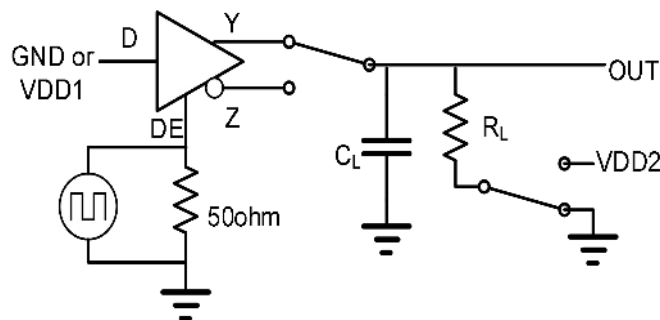


Figure 5.8 Driver Timing Test Circuit and waveform



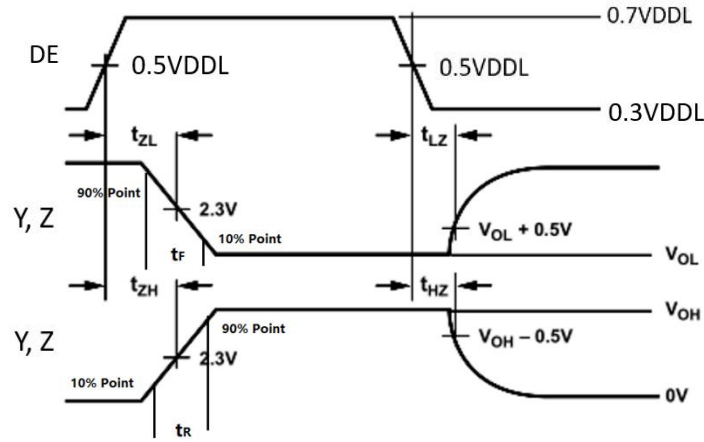


Figure5.9 Driver Enable Disable Timing Test Circuit and waveform

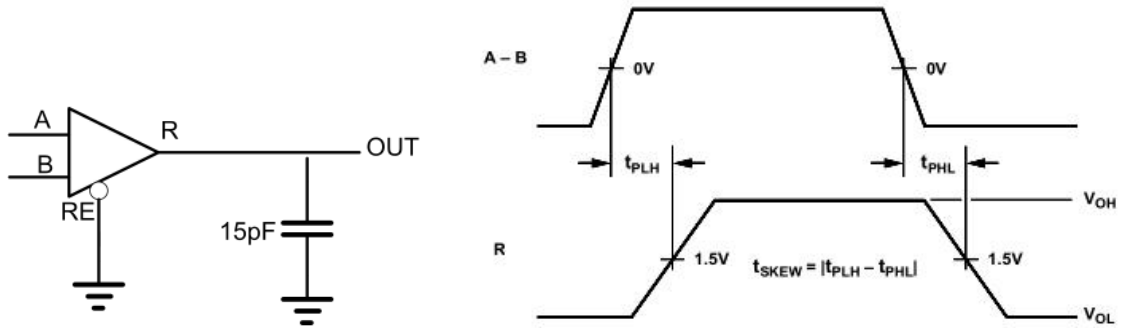


Figure 5.10 Receiver Propagation Delay Test Circuit and waveform

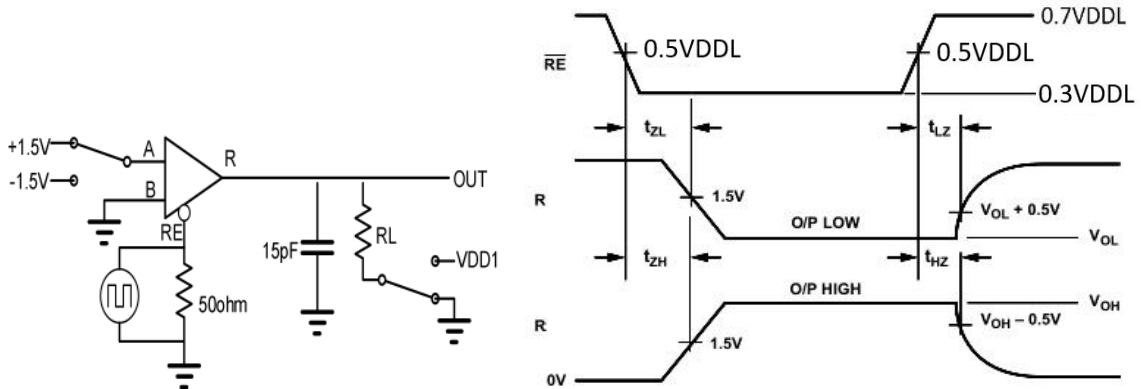


Figure 5.11 Receiver Enable Disable Timing Test Circuit and waveform

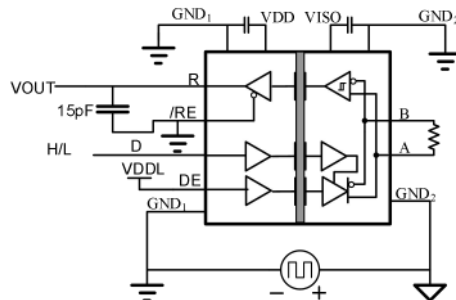


Figure5.12 Common-Mode Transient Immunity Test Circuit

## 6. High Voltage Feature Description

### 6.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Air Gap (Clearance)	CLR	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Distance through the insulation	DTI	16	um	Minimum internal gap (internal clearance – capacitive signal isolation)
		100	um	Minimum internal gap (internal clearance – transformer power isolation)
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		

### 6.2. DIN VDE V 0884-11 (VDE V 0884-11) :2017-01 INSULATION CHARATERISTICS

Description	Test Condition	Symbol	Value	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150Vrms			I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to IV	
For Rated Mains Voltage ≤ 600Vrms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive peak isolation voltage	AC voltage(bipolar)	$V_{IORM}$	1166	Vpeak
Maximum working isolation voltage	AC voltage(TDDb) test	$V_{IOWM}$	824	Vrms
	DC Voltage	$V_{IOWM}$	1166	V <sub>DC</sub>
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$ , 100%production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1749	Vpeak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial	$V_{pd(m)}$	1399	Vpeak

	discharge < 5 pC			
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1399	Vpeak
Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ ; $t = 60$ s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$ ; $t = 1$ s (100% production)	$V_{IOTM}$	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST} = 1.3 \times V_{ISOM}$	$V_{IOSM}$	5384	Vpeak
Isolation resistance	$V_{IO} = 500V$	$R_{IO}$	$>10^{12}$	$\Omega$
Isolation capacitance	$f = 1MHz$	$C_{IO}$	0.6	pF
Total Power Dissipation at 25 °C for SOW20 Package		$P_s$	1459	mW
Safety input, output, or supply current for SOW20 Package	$\theta_{JA} = 68.5^{\circ}C/W$ , $V_I = 5.5 V$ , $T_J = 125^{\circ}C$ , $T_A = 25^{\circ}C$	$I_s$	265	mA
Total Power Dissipation at 25 °C for SOW16 Package		$P_s$	1639	mW
Safety input, output, or supply current for SOW16 Package	$\theta_{JA} = 61^{\circ}C/W$ , $V_I = 5.5 V$ , $T_J = 125^{\circ}C$ , $T_A = 25^{\circ}C$	$I_s$	298	mA
Safety Temperature		$T_s$	125	$^{\circ}C$

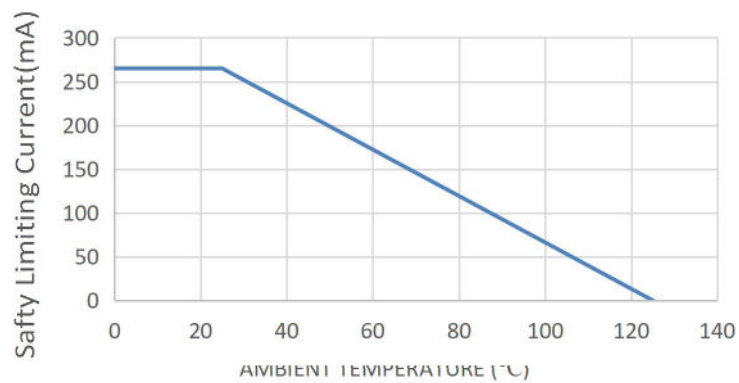


Figure 6.1 NSiP83086 Thermal Derating Curve for SOW20 package, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

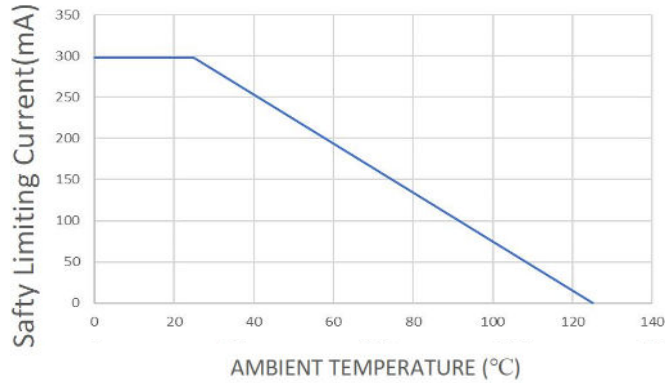


Figure 6.2 NSiP83086 Thermal Derating Curve for SOW16 package, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

### 6.3. Regulatory Information

The NSiP83086 are approved or pending approval by the organizations listed in table.

	<b>CUL</b>	<b>VDE</b>	<b>CQC</b>
UL 1577 Component Recognition Program <sup>1</sup>	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01 <sup>2</sup>	Certified by CQC11-471543-2012 GB4943.1-2022
Single Protection, 5000V <sub>RMS</sub> Isolation voltage	Single Protection, 5000V <sub>RMS</sub> Isolation voltage	Basic Insulation 1166V <sub>peak</sub> , V <sub>IOSM</sub> =5384V <sub>PEAK</sub>	Basic insulation
File (pending)	File (pending)	File (pending)	File (pending)

## 7. Function Description

NSiP83086 is a high reliability isolated full duplex RS-485 transceiver. Data isolation is achieved using Novosense integrated capacitive isolation that allows data transmission between the logic side and the Bus side. The 83086 series are safety certified by UL1577 supporting 5kV<sub>RMS</sub> insulation withstand voltage.

### 7.1. True Fail-Safe Receiver Inputs

The devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The receiver threshold is fixed between -10mV and -200mV, which meets EIA/TIA-485 standard. If the differential input voltage (V<sub>A</sub>-V<sub>B</sub>) is greater than or equal to -10mV, receiver output R is logic high. In the case of a terminated bus with all transmitters disabled, the differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold, the receiver output R is logic high.



### 7.2. Truth Tables

Table 7.1 Driver Function Table

<i>VDD<sub>1</sub></i> status	<i>Input (D)</i>	<i>Enable Input (DE)</i>	<i>Outputs</i>	
			<i>Y</i>	<i>Z</i>
PU	H	H	H	L
PU	L	H	L	H
PU	X	L	Z	Z
PU	X	OPEN	Z	Z
PU	OPEN	H	H	L
PD	X	X	Z	Z

Table 7.2 Receiver Function Table<sup>1</sup>

<i>VDD</i> status	<i>Differential Input (VA-VB)</i>	<i>Enable Input (/RE)</i>	<i>Output (R)</i>
PU	≥-10mV	L/Open	H
PU	≤-200mV	L/Open	L
PU	Open/Short	L/Open	H
PU	X	H	Z
PU	Idle	L	H
PD	X	X	Z

<sup>1</sup>PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance;

### 7.3. EMI Considerations

NSIP83086 use a small on-chip transformer to provide power for RS485 Transceiver. The on-chip transformer operates at high frequency, which may degrade EMI performance, to achieve better EMI performance, special considerations must be taken during PCB layout. Please see the application note if needed.

### 7.4. Output Short and Over Temperature Protection

The NSiP83086 series are protected against output short for  $V_{ISOOUT}$ . When short on  $V_{ISOOUT}$  occurs, the device will be in Hiccup mode and the power transferred will be limit, which will limit the temperature of the device to protect the device.

The NSiP83086 series also protected against over temperature. When the chip is over 165 °C, it will be shut down until the temperature of below 145 °C.

## 8. Application Note

### 8.1. 256 Transceivers on the Bus

The devices have a 1/8-unit-load receiver input impedance (96kΩ) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

### 8.2. ESD Protection

ESD protection structures are enhanced on all pins to protect against electrostatic discharge encountered during handling and assembly. The Bus pins have extra protection against static electricity to bus side ( $V_{ISOOUT}$  side).

ESD protection can be tested in various ways. Below is the ESD spec of the devices.

Bus pins:

- ±8kV using the Contact Discharge method specified in IEC 61000-4-2

Other pins except bus pins:

- ±7kV using the Contact Discharge method specified in IEC 61000-4-2

### 8.3. Layout Considerations

The NSiP83086 requires a 10μF+0.1μF bypass capacitor between  $VDD_1$  and  $GND_1$ , 10μF+0.1μF bypass capacitor between  $V_{ISOOUT}$  and  $GND_2$ . The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end (A-B, Y-Z) is terminated with a resistor, whose value matches the characteristic impedance of the cable(54 Ω /120 Ω ). It's good practice to place the bus connectors and termination resistor as close as possible to the A and B, Y and Z pins.

### 8.4. Typical Application

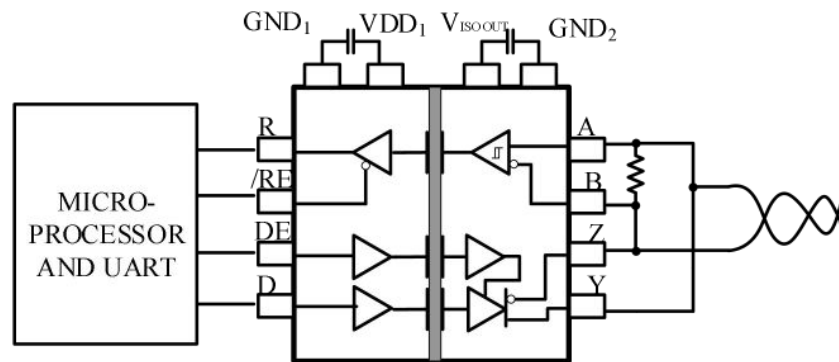


Figure 8.1 NSiP83086 in Half-Duplex RS-485 Mode

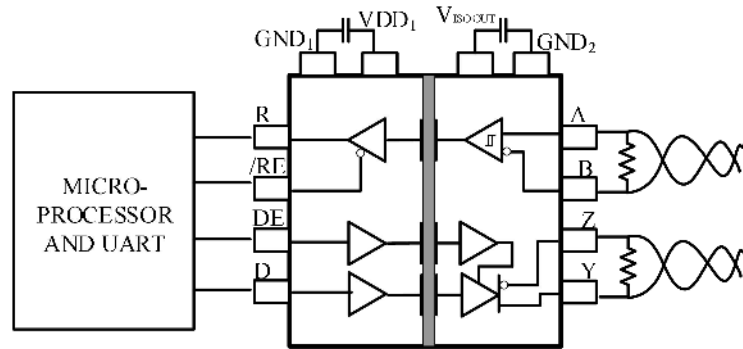


Figure 8.2 NSiP83086 typical application circuit

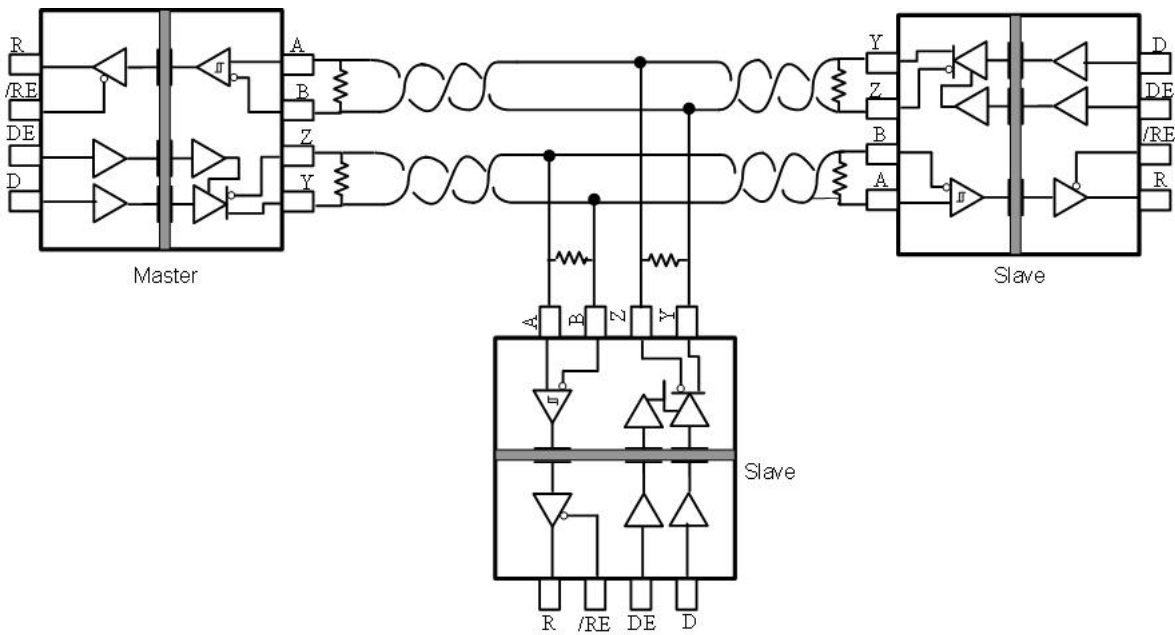


Figure 8.3 Typical isolated Full-Duplex RS-485 application

### 9. Package Information

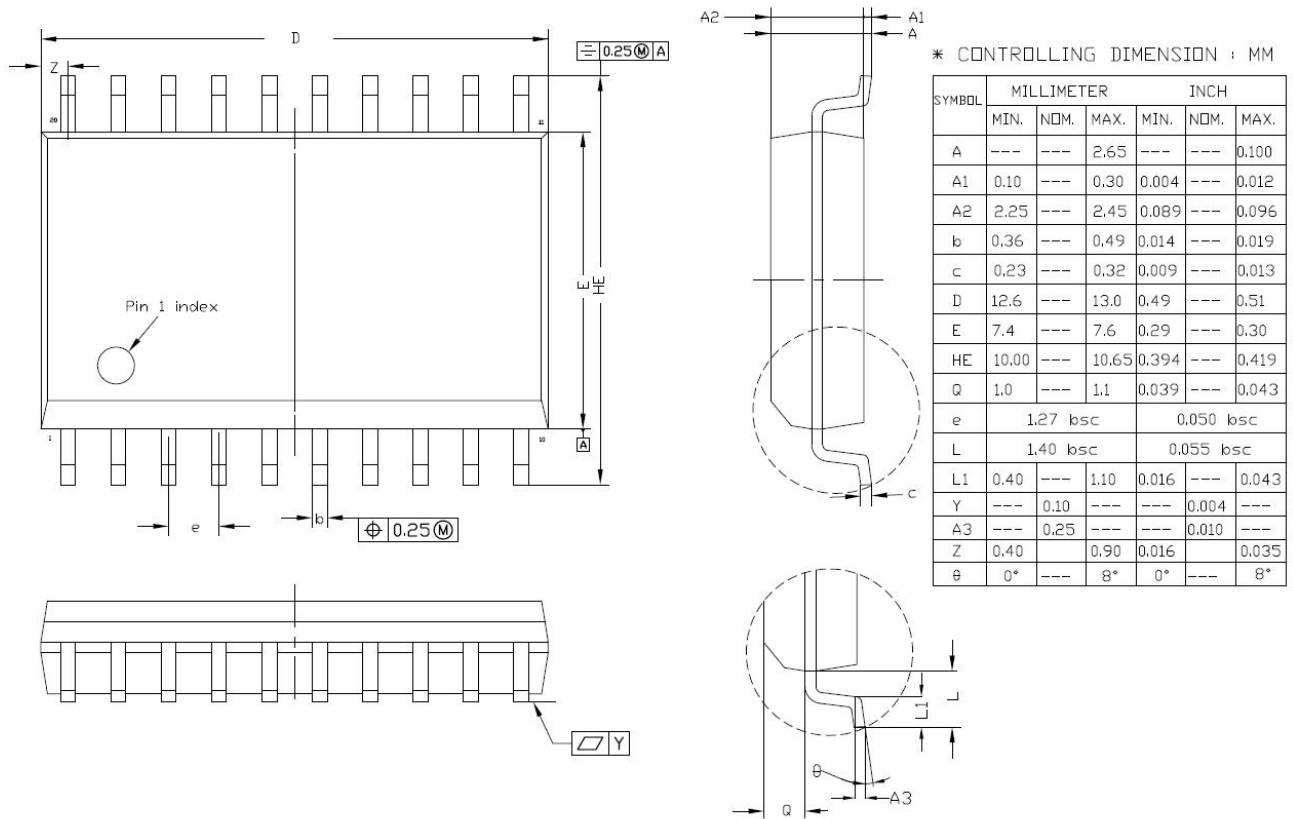


Figure 9.1 SOW20 Package Shape and Dimension in millimeters and inches

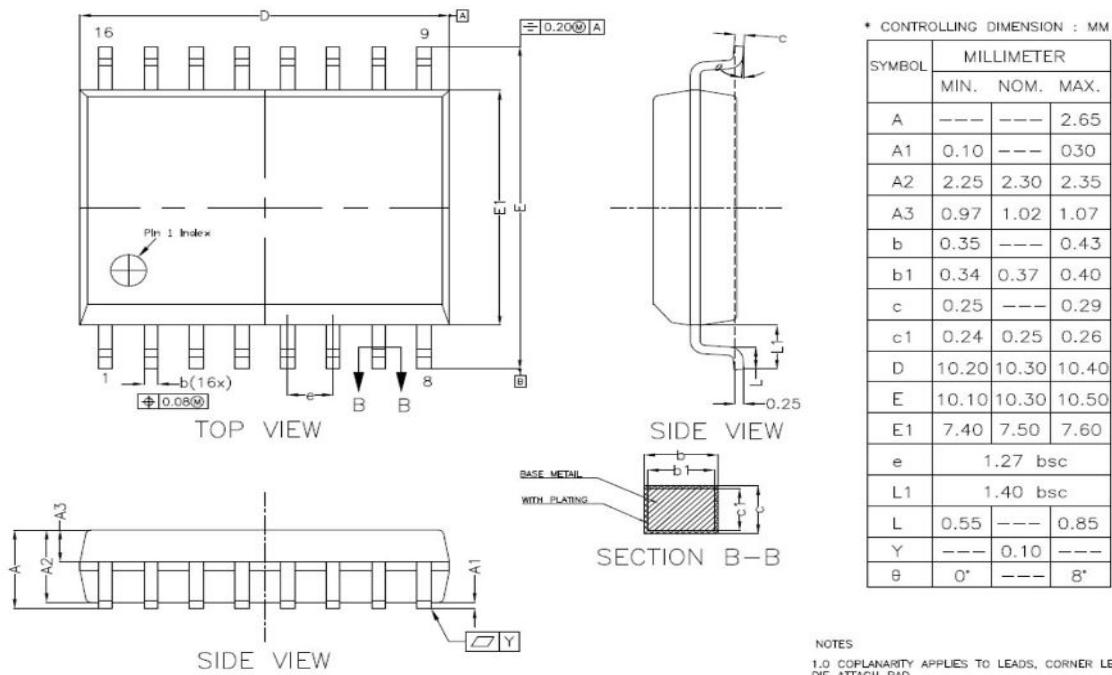


Figure 9.2 SOW16 Package Shape and Dimension in millimeters

### 10. Ordering Information

<b>Part Number</b>	<b>Isolation Rating (kV<sub>RMS</sub>)</b>	<b>V<sub>ISOOUT</sub></b>	<b>Duplex</b>	<b>Max Data Rate (Mbps)</b>	<b>MSL</b>	<b>Temperature</b>	<b>No. of Nodes</b>	<b>Package Type</b>	<b>Package Drawing</b>	<b>SPQ</b>
NSiP83086-DSWTR	5	5V	Full	16	3	-40 to 105°C	256	SOP20(300mil)	SOW20	1000
NSiP83086C-DSWTR	5	5/3.3V	Full	16	3	-40 to 105°C	256	SOP20(300mil)	SOW20	1000
NSiP83086V-DSWTR	5	3.3V	Full	16	3	-40 to 105°C	256	SOP20(300mil)	SOW20	1000
NSiP83086-DSWR	5	5V	Full	16	3	-40 to 105°C	256	SOP16(300mil)	SOW16	1000
NSiP83086V-DSWR	5	3.3V	Full	16	3	-40 to 105°C	256	SOP16(300mil)	SOW16	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

### 11. Documentation Support

<b>Part Number</b>	<b>Product Folder</b>	<b>Datasheet</b>	<b>Application Note</b>
NSiP83086	tbd	tbd	tbd

### 12. Tape And Reel Information

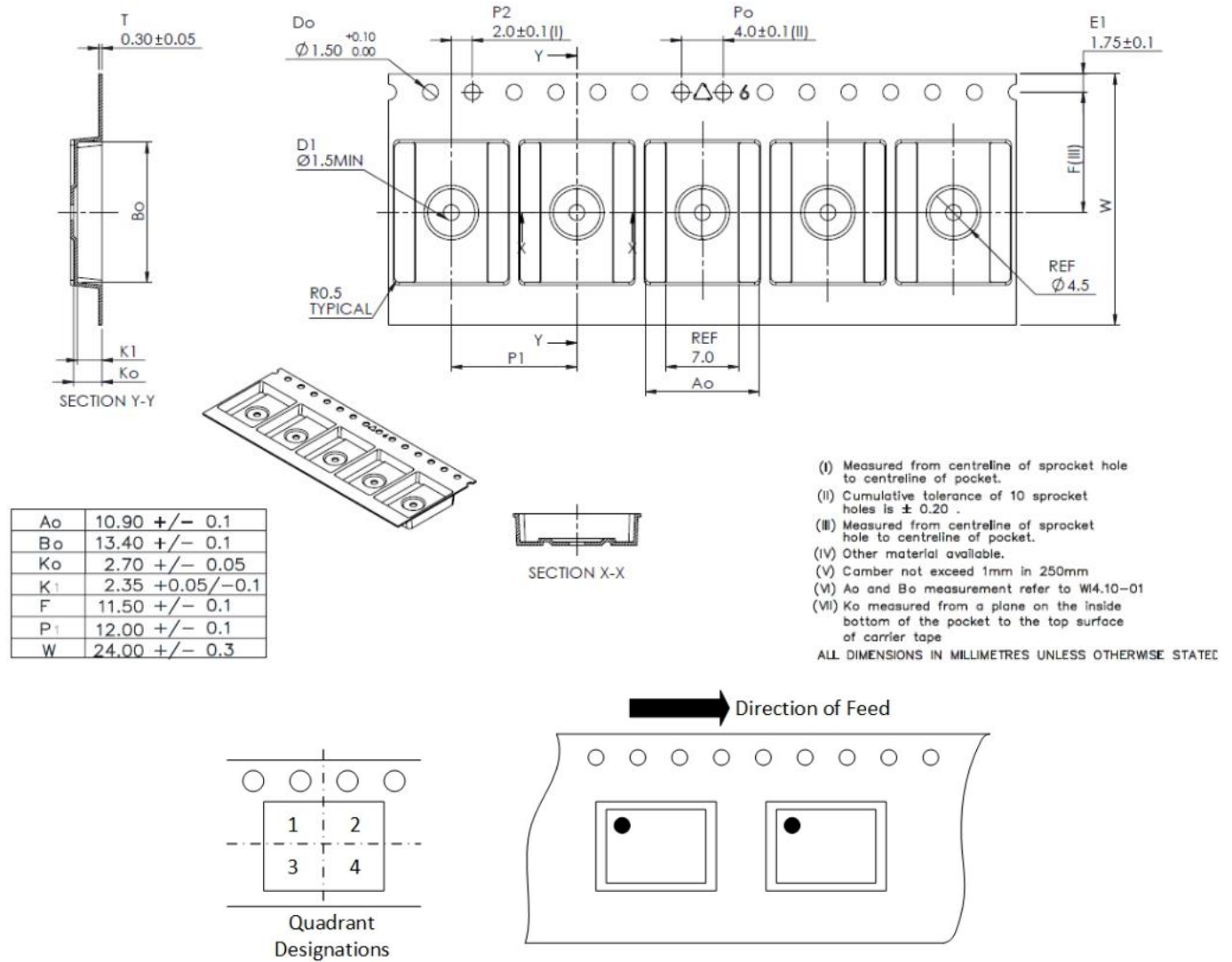
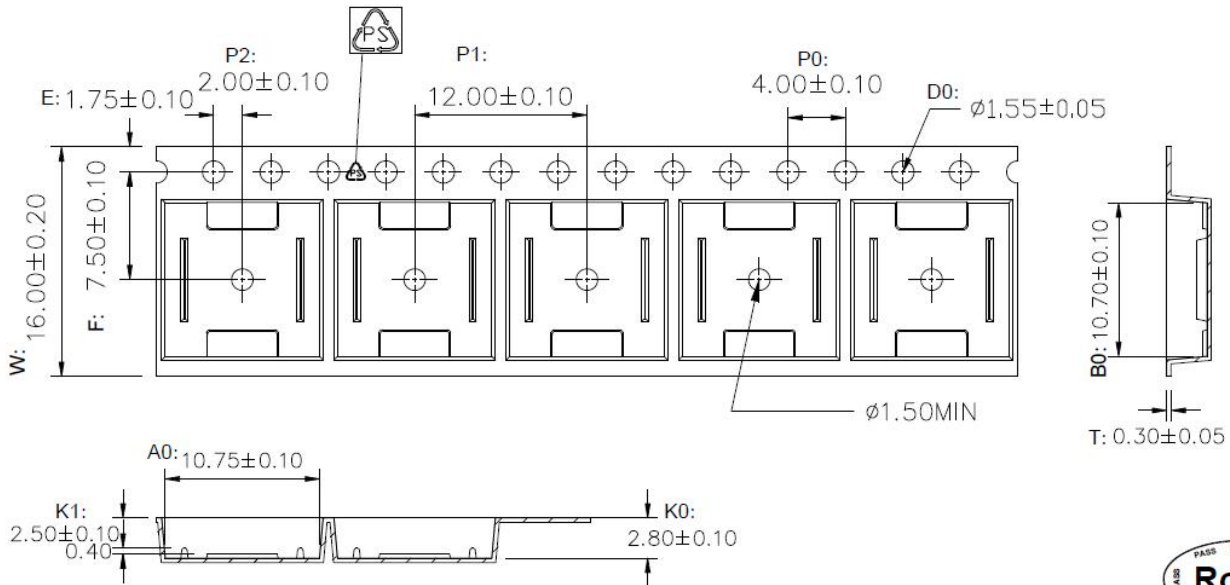


Figure 12.1 Tape and Reel Information of SOW20



1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$ .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness :  $0.30 \pm 0.05$ mm.
6. Packing length per 22" reel : 378 Meters.(復巻 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity :  $10^5 \sim 10^{10} \Omega/\square$



W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

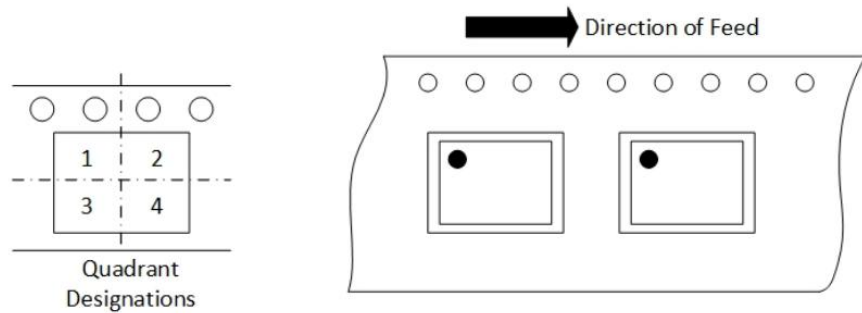


Figure 12.2 Tape and Reel Information of SOW16

### 13. Revision History

Revision	Description	Date
1.0	Initial Version	2022/11/30



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