NOVOSENSE
纳芯微电子

NSi8100

High Reliability Bidirectional I²C Isolators

Datasheet (EN) 2.3

Product Overview

The NSi8100 devices are high reliability bidirectional isolators that are compatible with I²C interface. The NSi8100 devices are safety certified by UL1577 support several insulation withstand voltages (3.75kV$_{rms}$, 5kV$_{rms}$), while providing high electromagnetic immunity and low emissions at low power consumption. The I²C clock of the NSi8100 is up to 2MHz, and the common-mode transient immunity (CMTI) is up to 150kV/us. Wide supply voltage of the NSi8100 device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 5000V$_{rms}$ Insulation voltage
- I²C Clock rate: up to 2MHz
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 150kV/us
- Chip level ESD: HBM: ±6kV
- High system level EMC performance:
  Enhanced system level ESD, EFT, Surge immunity
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  SOP8
  SOW16

Safety Regulatory Approvals

- UL recognition: up to 5000V$_{rms}$ for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Power over ethernet
- Isolated I²C, SMBus, or PMBus interface
- I²C level shifting
- Battery Management

Device Information

Part Number	*Package*	*Body Size*
NSi8100N	SOP8	6.00mm × 5.00mm
NSi8100W	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

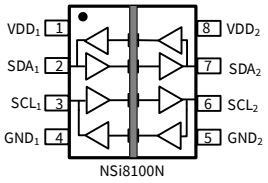

Figure 1. NSi8100N Block Diagram

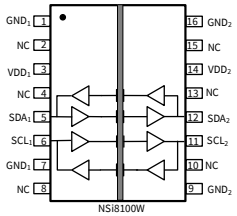

Figure 2. NSi8100W Block Diagram

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1. Package Information

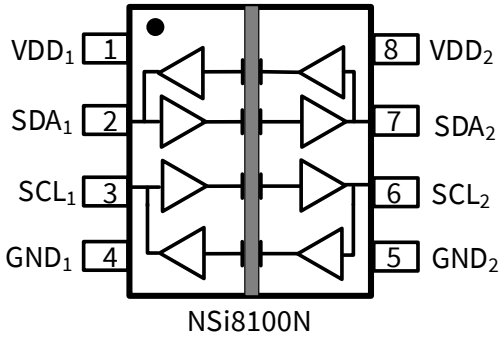


Figure 1.1 NSi8100N Package

Table1.1 NSi8100N Pin Configuration and Description

NSi8100N PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD_1	Power Supply for Isolator Side 1
2	SDA_1	Serial data input /output, Side 1
3	SCL_1	Serial clock input /output, Side 1
4	GND_1	Ground 1, the ground reference for Isolator Side 1
5	GND_2	Ground 2, the ground reference for Isolator Side 2
6	SCL_2	Serial clock input /output, Side 2
7	SDA_2	Serial data input /output, Side 2
8	VDD_2	Power Supply for Isolator Side 2

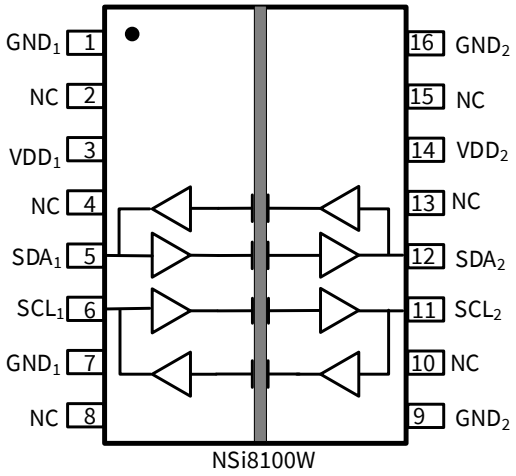


Figure 1.2 NSi8100W Package

Table1.2 NSi8100W Pin Configuration and Description

NSi8100W PIN NO.	*SYMBOL*	*FUNCTION*
1	GND_1	Ground 1, the ground reference for Isolator Side 1
2	NC	No Connection.
3	VDD_1	Power Supply for Isolator Side 1
4	NC	No Connection.
5	SDA_1	Serial data input /output, Side 1
6	SCL_1	Serial clock input /output, Side 1
7	GND_1	Ground 1, the ground reference for Isolator Side 1
8	NC	No Connection.
9	GND_2	Ground 2, the ground reference for Isolator Side 2
10	NC	No Connection.
11	SCL_2	Serial clock input /output, Side 2
12	SDA_2	Serial data input /output, Side 2
13	NC	No Connection.
14	VDD_2	Power Supply for Isolator Side 2
15	NC	No Connection.
16	GND_2	Ground 2, the ground reference for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	SDA_1, SDA_2, SCL_1, SCL_2	-0.4		VDD+0.4[1]	V	
Maximum Input Pulse Voltage	SDA_1, SDA_2, SCL_1, SCL_2	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	Io	-15		15	mA	
Maximum Surge Isolation Voltage	V_{IOSM}			5.3	kV	
Operating Temperature	Topr	-40		125	℃	
Junction Temperature	T_j			150	℃	
Storage Temperature	Tstg	-65		150	℃	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	Topr	-40		125	℃
Side1 High Level Input Voltage	VIH1	0.6			V
Side1 Low Level Input Voltage	VIL1			0.4	V
Side2 High Level Input Voltage	VIH2	V_{DD2}*0.7			
Side2 Low Level Input Voltage	VIL2			V_{DD2}*0.3	
Data rate	DR	0		2	Mbps

4. Thermal Characteristics

Parameters	Symbol	SOW16	SOP8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	86.5	137.7	℃/W

Parameters	Symbol	SOW16	SOP8	Unit
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	49.6	54.9	℃/W
Junction-to-board thermal resistance	θ_{JB}	49.7	71.7	℃/W

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
Start Up Time after POR	trbs		40		usec	
Common Mode Transient Immunity	CMTI	±100	±150		kV/us	See figure 5.8
SDA, SCL logic low leakage	IIL			15	uA	
Side 1 Logic Level						
Input Threshold	V_{ILT1}	400			mV	Input Threshold at falling edge
	V_{IHT1}			600	mV	Input Threshold at rising edge
	V_{IT_HYS1}		100		mV	Input Threshold Hysteresis
Low Level Output Voltage	V_{OL1}	650		800	mV	I_{OL} ≤ 4mA， $R_{PULL\ UP}$=1K
Low-level output voltage to high-level input voltage threshold difference	ΔV_{OIT1}	70			mV	
Side 2 Logic Level						
High Level Input Voltage	V_{IH2}	V_{DD2}*0.7			V	
Low Level Input Voltage	V_{IL2}			V_{DD2}*0.3	V	
Low Level Output Voltage	V_{OL}			0.5	V	I_{OL} ≤ 30mA

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I_{DD1}(Q0)		5.10	7.5	mA	All Input 0V

	I_{DD2}(Q0)		3.96	5.7	mA	
	I_{DD1}(Q1)		2.52	3.6	mA	All Input at supply
	I_{DD2}(Q1)		1.78	2.5	mA	
	I_{DD1}(2M)		3.83	5.7	mA	All Input with 2MHz, C_L=15pF
	I_{DD2}(2M)		2.78	4.2	mA	
Clock rate	DR	0		2	MHz	
Propagation Delay	t_{PLH12}		24.8	37.2	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD
	t_{PHL12}		32.8	49.2	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD
	t_{PLH21}		24	36	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD
	t_{PHL21}		38	57	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD
Pulse Width Distortion	PWD_{12}		8	12	ns	$\lvert t_{PHL12} - t_{PLH12} \rvert$
	PWD_{21}		14	21	ns	$\lvert t_{PHL21} - t_{PLH21} \rvert$
Falling Time	t_{f1}		10.6	15.9	ns	C_L = 30pF
	t_{f2}		22.8	34.2	ns	C_L = 300pF

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25℃)

Parameters	***Symbol***	***Min***	***Typ***	***Max***	***Unit***	***Comments***
	I_{DD1}(Q0)		4.96	7.4	mA	All Input 0V
	I_{DD2}(Q0)		3.85	5.6	mA	
	I_{DD1}(Q1)		2.40	3.5	mA	All Input at supply
	I_{DD2}(Q1)		1.68	2.4	mA	
	I_{DD1}(2M)		3.69	5.6	mA	All Input with 2MHz, C_L=15pF
	I_{DD2}(2M)		2.67	4.2	mA	
Clock rate	DR	0		2	MHz	
Propagation Delay	t_{PLH12}		29	43.5	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD
	t_{PHL12}		39.8	59.7	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD

	t_{PLH21}		30	45	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD
	t_{PHL21}		61	91.5	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD
Pulse Width Distortion	PWD_{12}		10.8	16.2	ns	$\lvert t_{PHL12} - t_{PLH12} \rvert$
	PWD_{21}		31	46.5	ns	$\lvert t_{PHL21} - t_{PLH21} \rvert$
Falling Time	t_{f1}		15.6	23.4	ns	C_L = 30pF
	t_{f2}		32	48	ns	C_L = 300pF

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
	I_{DD1}(Q0)		4.89	7.3	mA	All Input 0V
	I_{DD2}(Q0)		3.79	5.5	mA	
	I_{DD1}(Q1)		2.34	3.4	mA	All Input at supply
	I_{DD2}(Q1)		1.63	2.3	mA	
	I_{DD1}(2M)		3.61	5.4	mA	All Input with 2MHz, C_L=15pF
	I_{DD2}(2M)		2.59	4	mA	
Clock rate	DR	0		2	MHz	
Propagation Delay	t_{PLH12}		33	49.5	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD
	t_{PHL12}		52	78	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD
	t_{PLH21}		47	70.5	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD
	t_{PHL21}		100	150	ns	See figure 5.7, R1=1500Ω, R2=500Ω, NO LOAD
Pulse Width Distortion	PWD_{12}		19	28.5	ns	$\lvert t_{PHL12} - t_{PLH12} \rvert$
	PWD_{21}		53	79.5	ns	$\lvert t_{PHL21} - t_{PLH21} \rvert$
Falling Time	t_{f1}		22	33	ns	C_L = 30pF
	t_{f2}		36	54	ns	C_L = 300pF

5.2. Typical Performance Characteristics

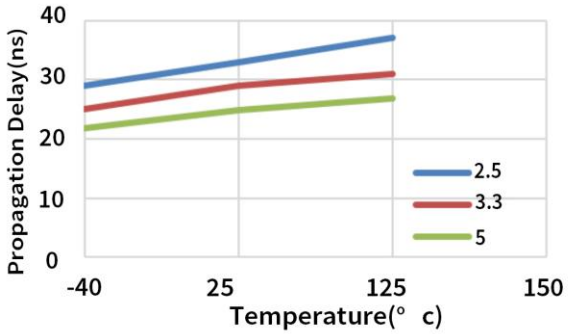


Figure 5.1 Side1 to Side2 Rising Edge Propagation Delay Vs Temp

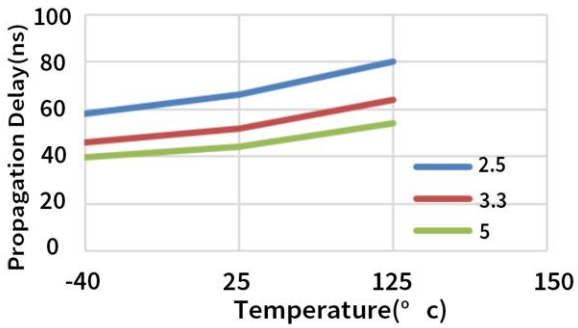


Figure 5.2 Side1 to Side2 Falling Edge Propagation Delay Vs Temp

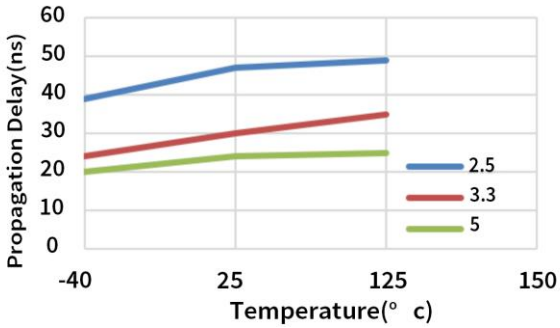


Figure 5.3 Side2 to Side1 Rising Edge Propagation Delay Vs Temp

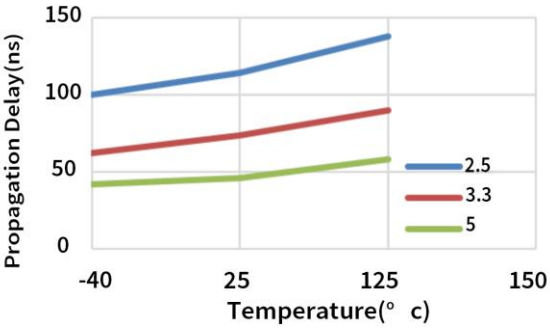


Figure 5.4 Side2 to Side1 Falling Edge Propagation Delay Vs Temp

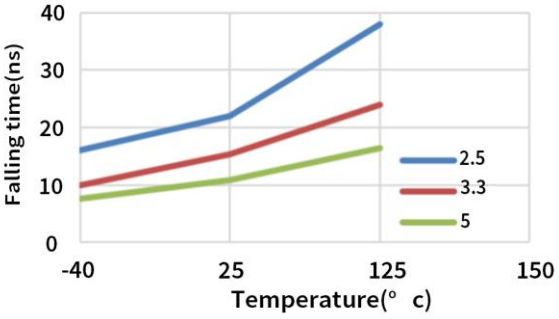


Figure 5.5 Falling time(@27pF) Vs Temp

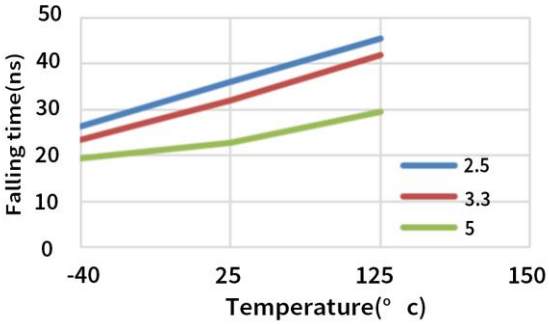


Figure 5.6 Falling time(@300pF) Vs Temp

5.3. Parameter Measurement Information

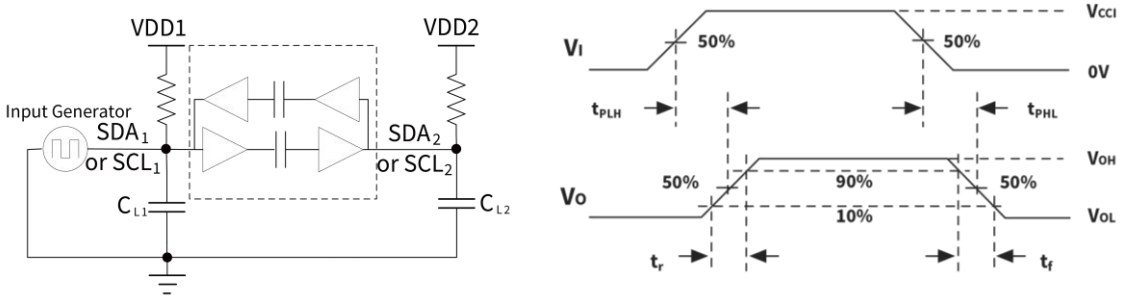


Figure 5.7 Switching Characteristic Test Circuit and Voltage Waveforms

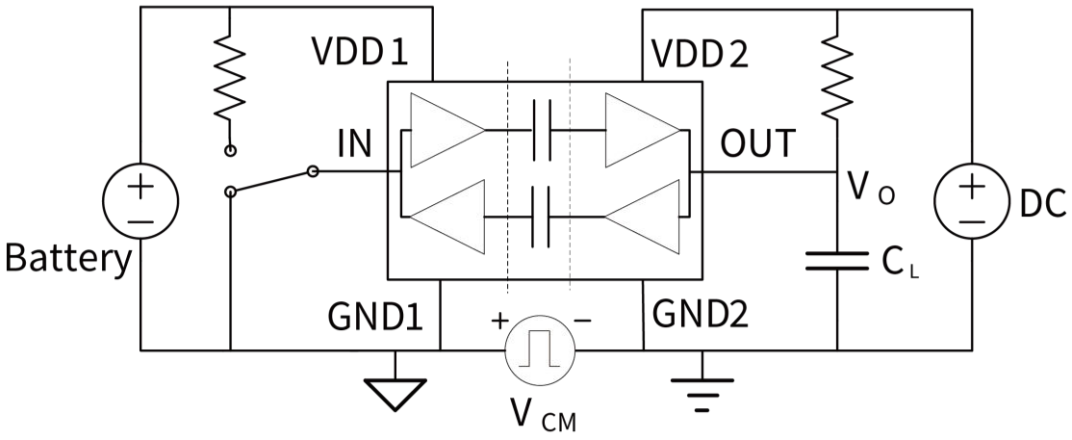


Figure 5.8 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
			SOP8	SOW16	
Minimum External Air Gap (Clearance)		L(I01)	4.0	8.0	mm
Minimum External Tracking (Creepage)		L(I02)	4.0	8.0	mm
Distance through the Insulation		DTI	20		um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>400		V
Material Group	IEC 60112		II		
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150V_{rms}			I to IV	I to IV	
For Rated Mains Voltage ≤ 300V_{rms}			I to III	I to IV	
For Rated Mains Voltage ≤ 400V_{rms}			I to III	I to IV	
Insulation Specification per DIN VDE V 0884-11:2017-01[1)]					
Climatic Classification			10/105/21	10/105/21	
Pollution Degree	per DIN VDE 0110, Table 1		2	2	
Maximum repetitive isolation voltage		V_{IORM}	565	1166	Vpeak
Maximum working isolation voltage	AC	V_{IOWM}	400	824	Vrms
	DC		565	1166	Vpeak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	847	1749	Vpeak

Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	678	1399	Vpeak
Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	678	1399	Vpeak
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	5300	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST}=1.3\times V_{IOSM}$	V_{IOSM}	5384	5384	Vpeak
Isolation resistance	V_{IO} =500V	R_{IO}	>10^9	>10^9	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.6	0.6	pF
Insulation Specification per UL1577					
Withstand Isolation Voltage	$V_{TEST} = 1.2 \times V_{ISO}$, t = 1 sec, 100% production test	V_{ISO}	3750	5000	V_{rms}

1) This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

6.2. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSi8100N(SOP8)

Description	*Test Condition*	*Value*	*Unit*
Safety Supply Power	$R_{\theta JA}$ = 137.7°C/W[1)], T_J = 150 °C, T_A = 25 °C	907	mW
Safety Supply Current	$R_{\theta JA}$ = 137.7°C/W[1)], V_I = 5V, T_J = 150 °C, T_A = 25 °C	181	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8 package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

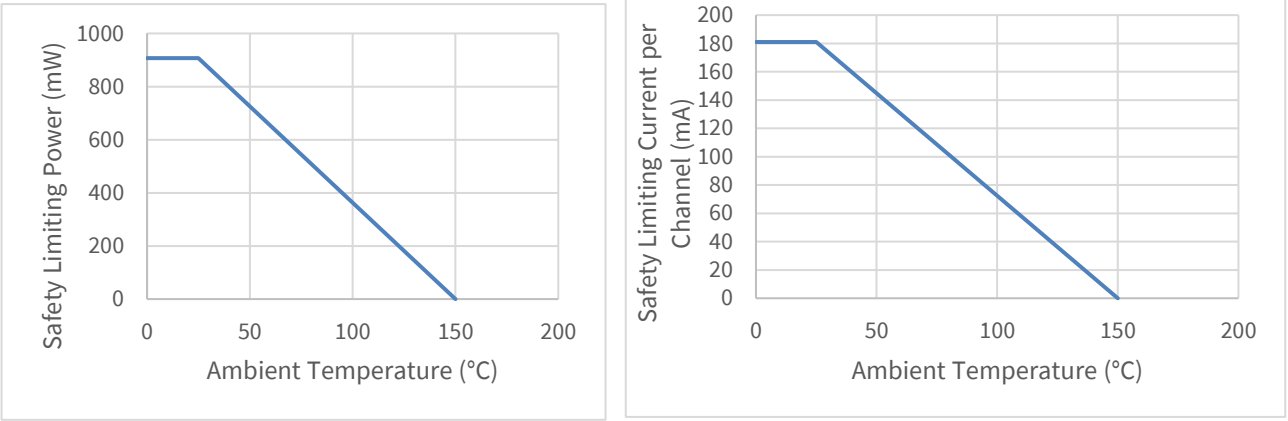


Figure 6.1 NSi8100N Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSi8100W(SOW16)

Description	*Test Condition*	*Value*	*Unit*
Safety Supply Power	$R_{\theta JA}$ = 86.5°C/W[1)], T_J = 150 °C, T_A = 25 °C	1445	mW
Safety Supply Current	$R_{\theta JA}$ = 86.5°C/W[1)], V_I = 5V, T_J = 150 °C, T_A = 25 °C	289	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOW16 package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

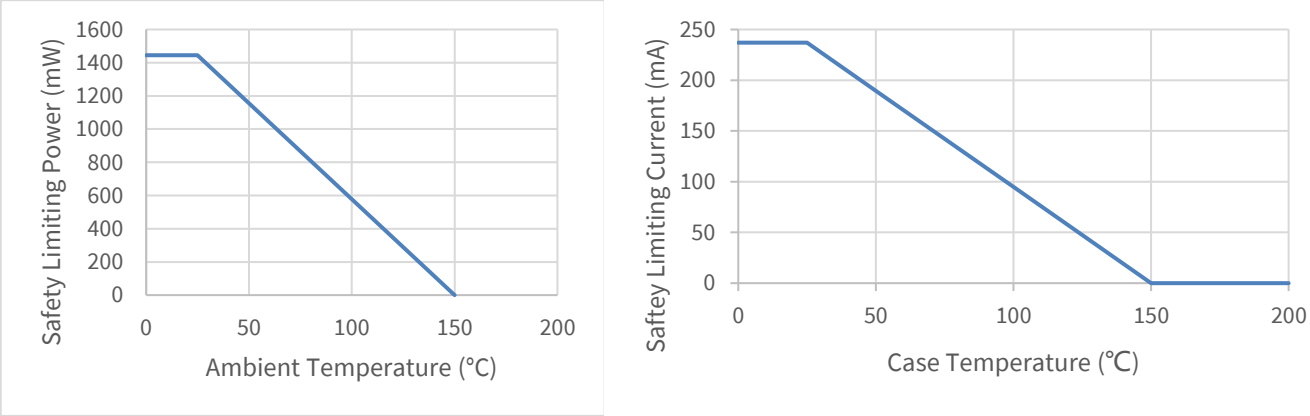


Figure 6.2 NSi8100W Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NSi8100N are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750V_{rms} Isolation voltage	Single Protection, 3750V_{rms} Isolation voltage	Basic Insulation 565Vpeak, V_{IOSM}=5384Vpeak	Basic insulation
File (E500602)	File (E500602)	File (5024579-4880-0001)	File (pending)

The NSi8100W are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Basic Insulation 849Vpeak, V_{IOSM}=5384Vpeak	Basic insulation
File (E500602)	File (E500602)	File (5024579-4880-0001)	File (pending)

7. Function Description

The NSi8100 is a bidirectional isolator based on a capacitive isolation barrier technique. The NSi8100 devices are compatible with I^2C interface. Internally, the I^2C interface is split into two unidirectional channels communicating in opposing directions via a dedicate capacitive isolation channel for each. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi8100 devices are high reliability dual-channel bidirectional isolators for clock and data lines. The NSi8100 is suitable for multi-master application.

The Side 2 logic levels of NSi8100 are standard I^2C value, and the maximum load for side 2 is ≤ 400pF. So multiple NSi8100 devices connected to a bus by their Side 2 pins can communicate with each other and with other I^2C compatible devices.

The Side 1 logic levels of NSi8100 are not standard value. The output low level of NSi8100 is 650mV, while low-level output voltage to high-level input voltage threshold is 50mV. This prevents an output logic low at Side 1 being transmitted back to Side 2 and pulling down the I^2C bus.

The NSi8100 device is safety certified by UL1577 support several insulation withstand voltages (3.75kV$_{rms}$, 5kV$_{rms}$), while providing high electromagnetic immunity and low emissions at low power consumption. The I^2C clock of the NSi8100 is up to 2MHz, and the common-mode transient immunity (CMTI) is up to 150kV/us. Wide supply voltage of the NSi8100 device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

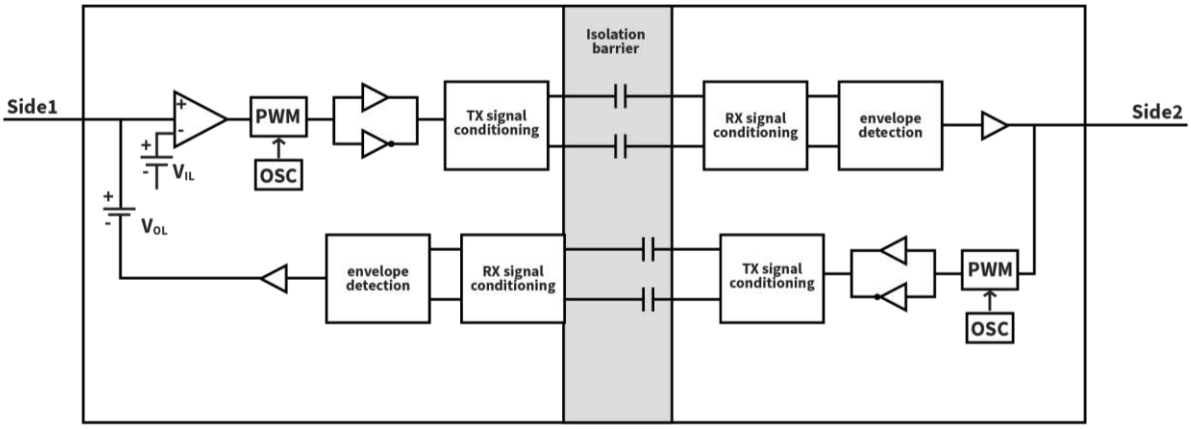


Figure 7.1 Simplified Channel Diagram

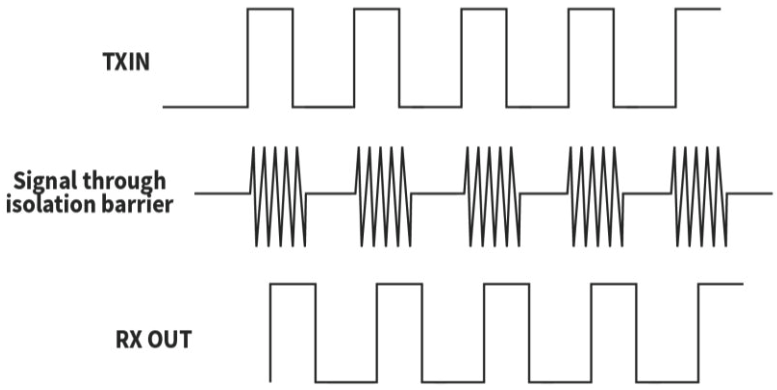


Figure 7.2 OOK Based Modulation Scheme

The Table 7.1 shows the functional of NSi8100.The NSi8100 is high impedance output when VDDIN is unready and VDDOUT is ready as shown in.

Table 7.1 Output status vs. power status

Input	*VDD1 status*	*VDD2 status*	*Output*	*Comment*
H	Ready	Ready	Z	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	Z	The output follows the same status with the input within 60us after input side VDD1 is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 60us after output side VDD2 is powered on.

8. Application Note

8.1. PCB Layout

The NSi8100 requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 8.1 to Figure 8.4 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. The pull-up resistors required for both Side 1 and Side 2 buses. And the value of the resistors depend on the number of I^2C devices on the bus.

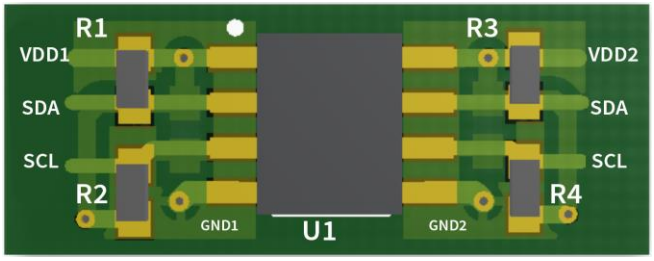


Figure8.1 Recommended PCB Layout — Top Layer

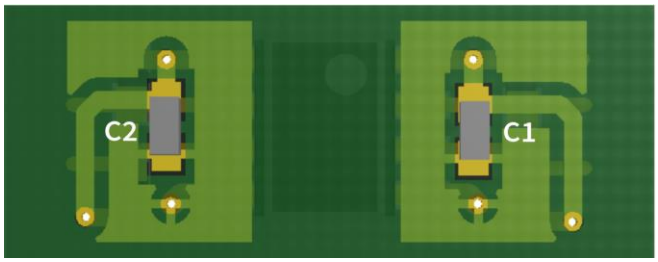


Figure8.2 Recommended PCB Layout — Bottom Layer

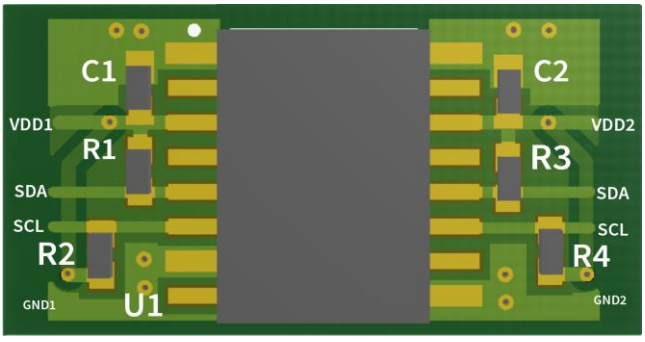


Figure8.3 Recommended PCB Layout — Top Layer

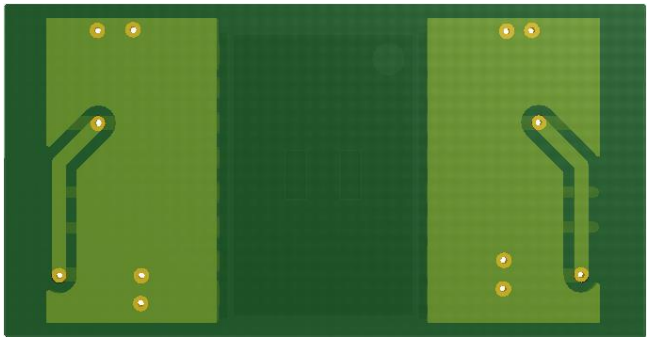
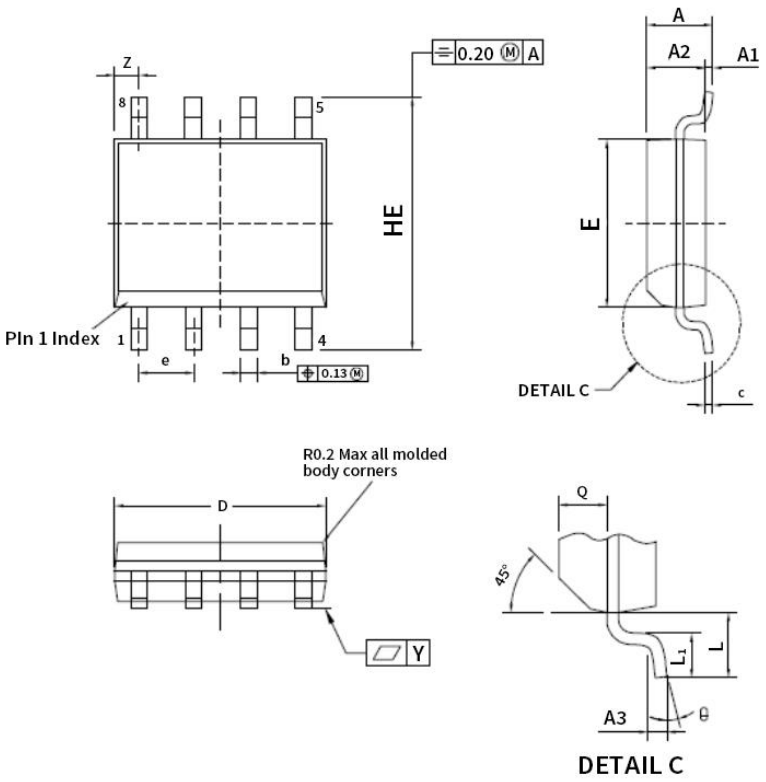


Figure8.4 Recommended PCB Layout — Bottom Layer

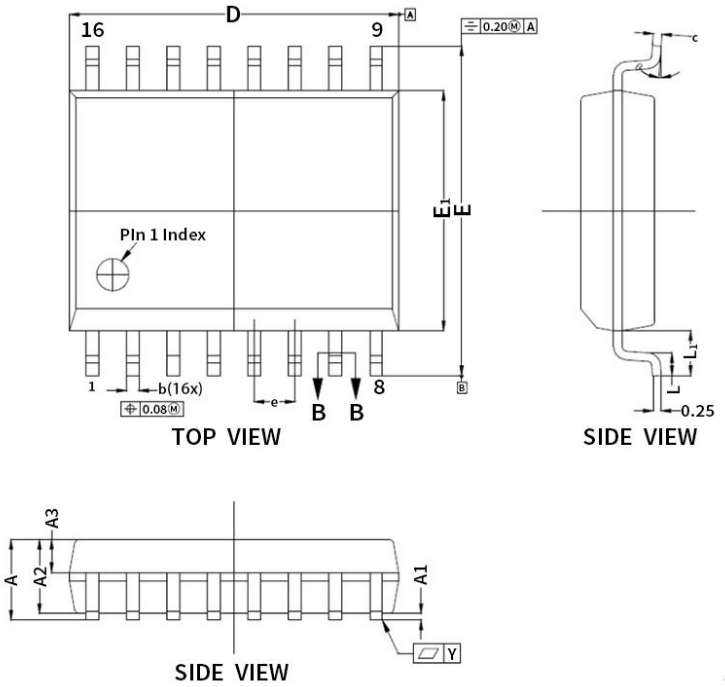
9. Package Information



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

Figure 9.1 SOP8 Package Shape and Dimension in millimeters



* CONTROLLING DIMENSION:MM

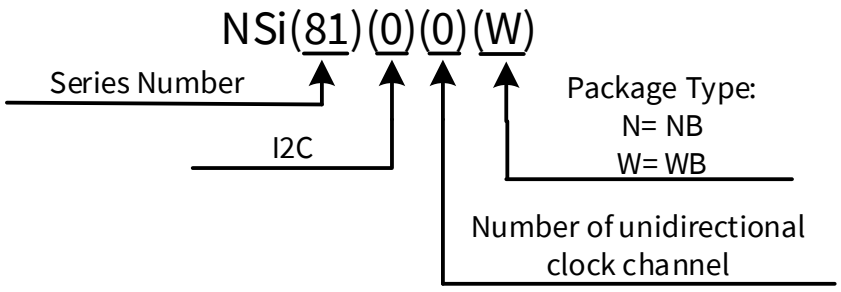
SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 9.2 SOW16 Package Shape and Dimension in millimeters

10. Order Information

Part No.	*Isolation Rating(kV)*	*Number of side 1 inputs*	*Number of side 2 inputs*	*Max Clock Rate (MHz)*	*Operating Temperature*	*MSL*	*Automotive*	*Package*	*SPQ*
NSi8100N	3.75	2	2	2	-40 to 125℃	1	NO	SOP8	2500
NSi8100W	5	2	2	2	-40 to 125℃	2	NO	SOW16	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 ℃ according to the JEDEC industry standard classifications and peak solder temperatures.									

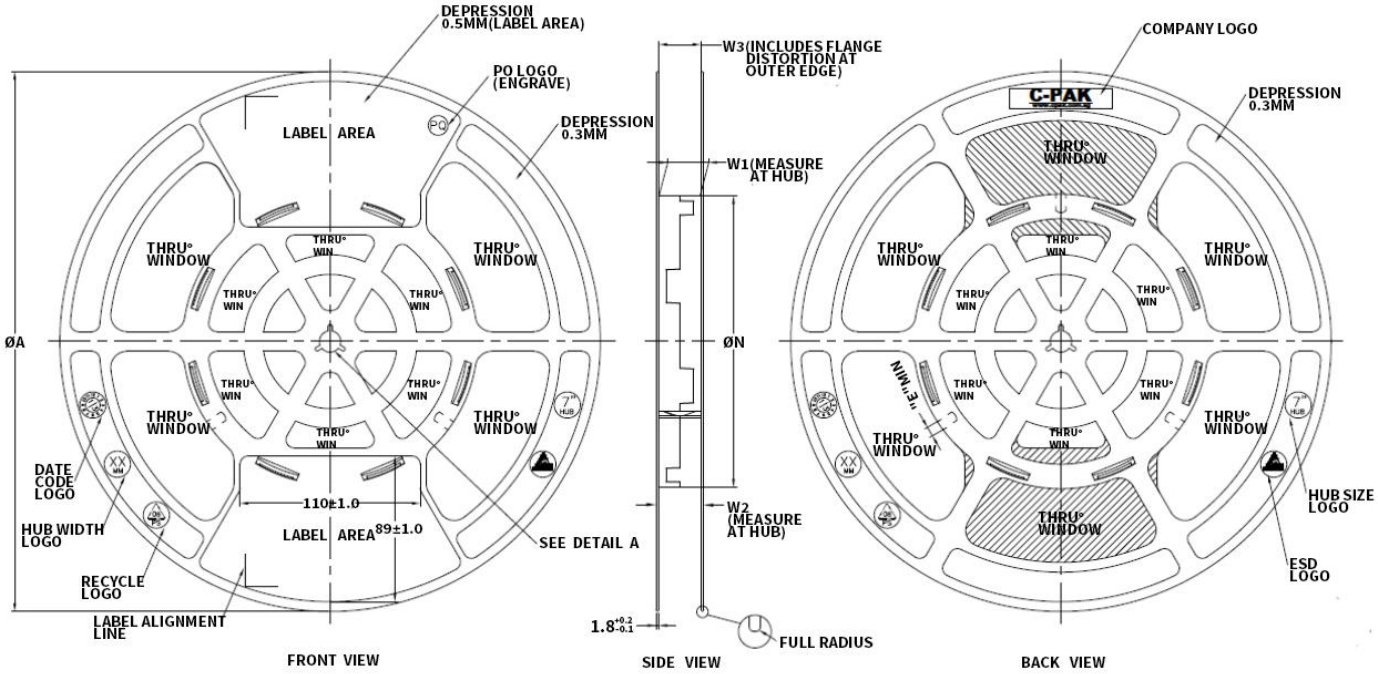
Part Number Rule:

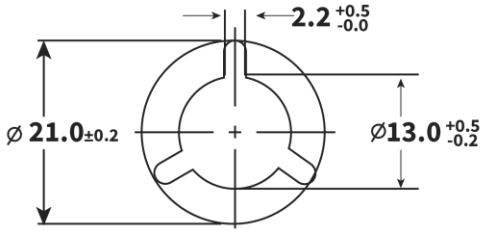


11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSi8100	tbd	tbd	tbd	tbd

12. Tape and Reel Information

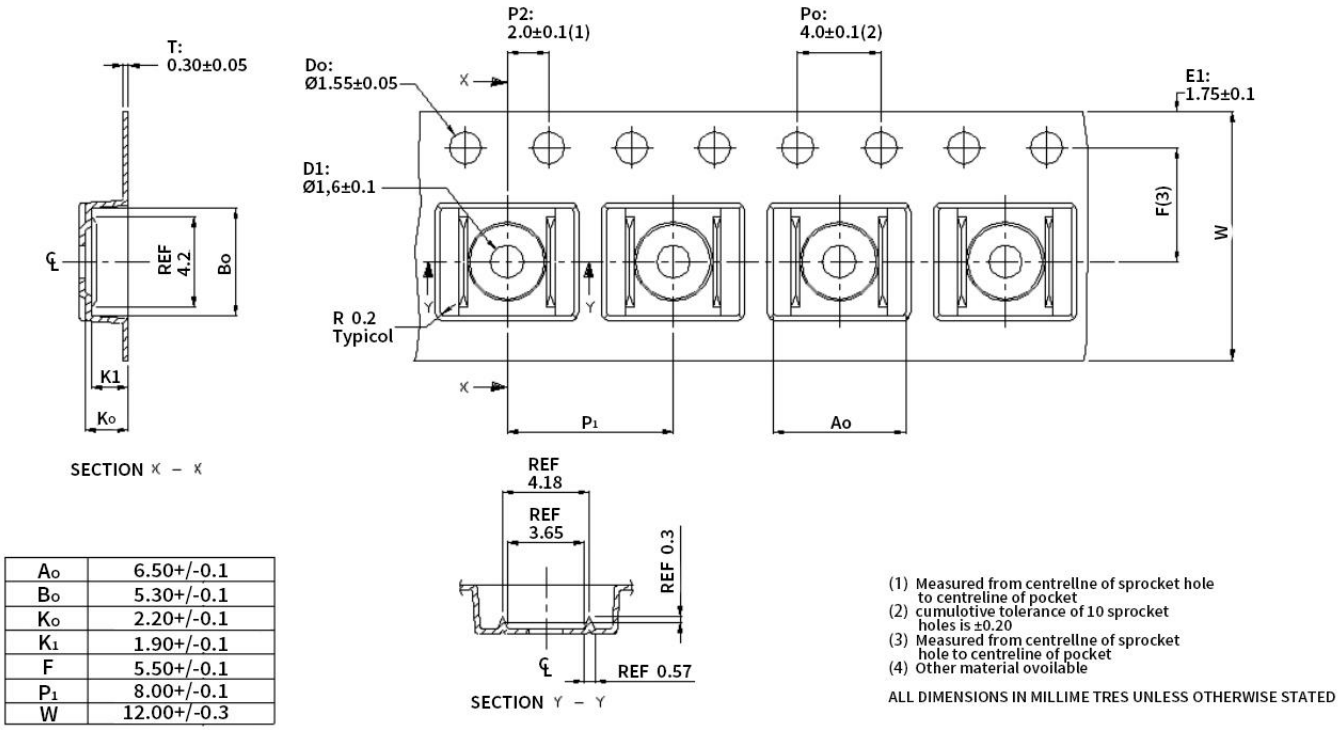




ARBOR HOLE
DETAIL A
SCALE: 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES



A_o	6.50+/-0.1
B_o	5.30+/-0.1
K_o	2.20+/-0.1
K_1	1.90+/-0.1
F	5.50+/-0.1
P_1	8.00+/-0.1
W	12.00+/-0.3

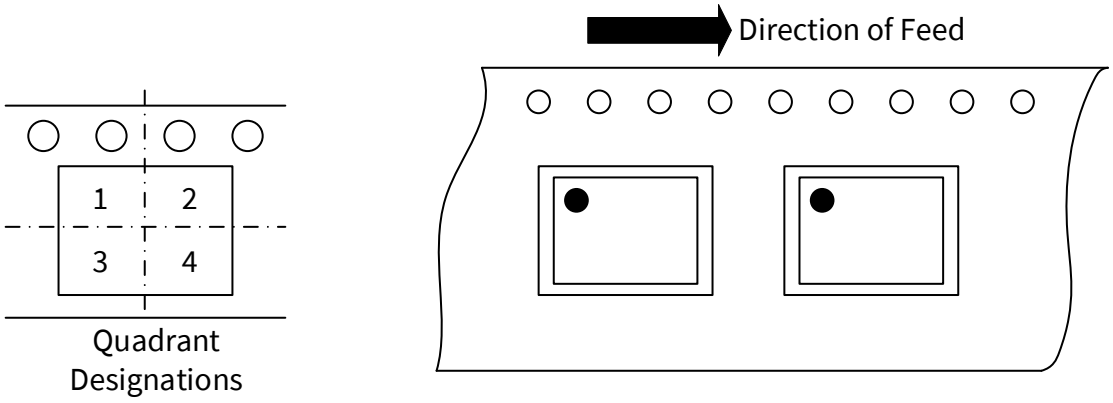
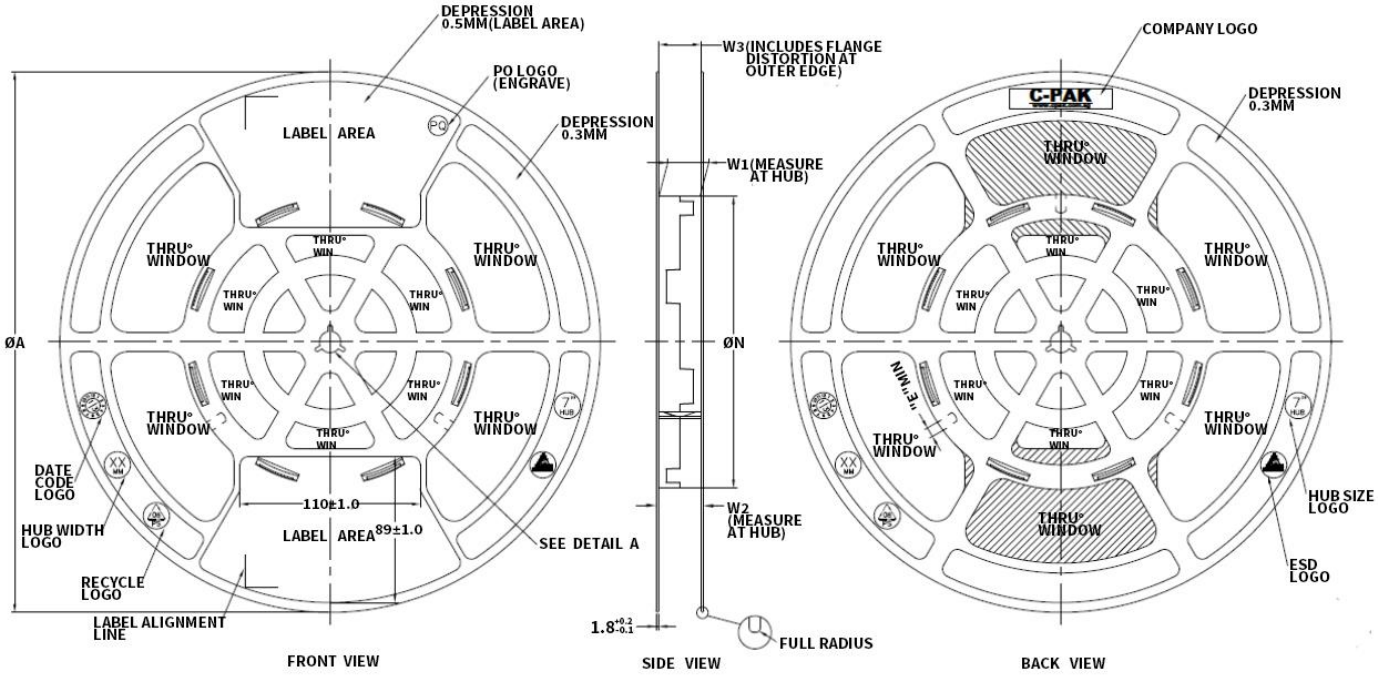
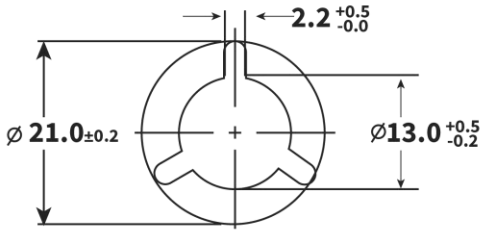


Figure 11.1 Tape and Reel Information of SOP8

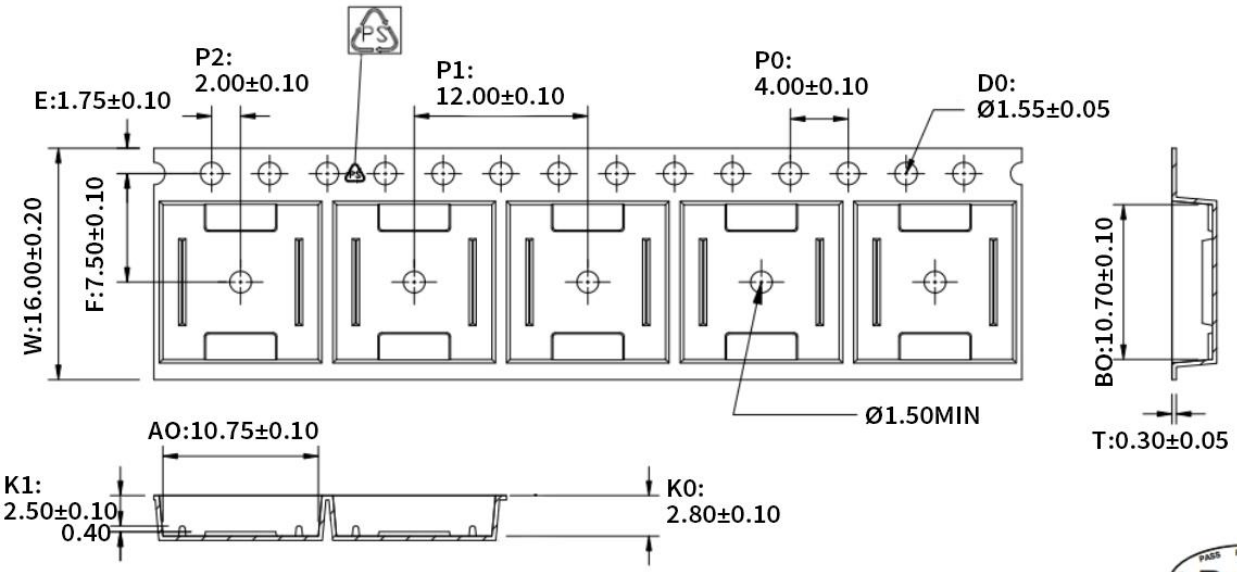




ARBOR HOLE
DETAIL A
SCALE: 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES



1.10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30±0.05mm.
6. Packing length per 22" reel: 378 Meters.(Rewind N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:10^{5}~ $10^{10}\Omega/\square$

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

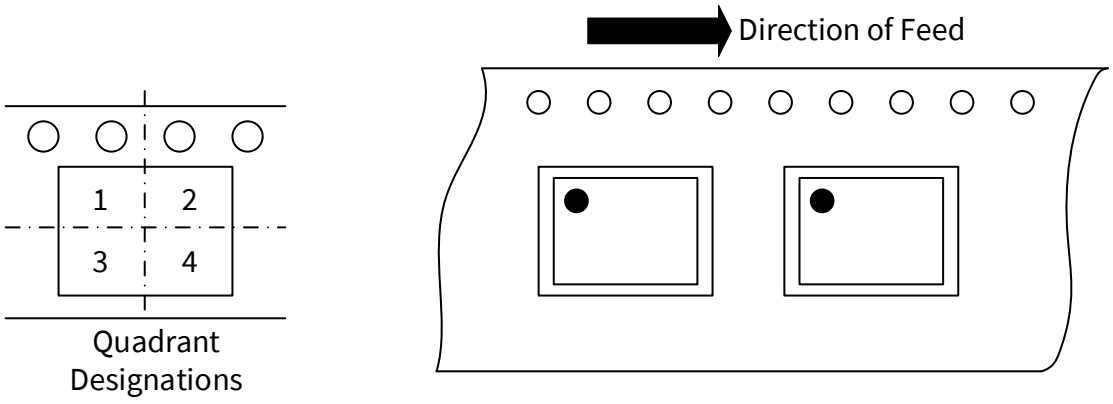


Figure 11.2 Tape and Reel Information of SOW16

13. Revision History

Revision	Description	Date
1.0	Original	2017/11/15
1.1	Change to Ordering information	2018/3/26
1.2	Add maximum operation current specification.	2018/6/20
1.3	Change block diagram	2018/7/28
1.4	Change “Start Up Time after POR” specification to 40us	2018/8/25
1.5	Add “Maximum Input Pulse Voltage”	2018/10/9
1.6	Change to Ordering information	2018/12/20
1.7	Change Certification Information, Add “SDA,SCL logic low leakage”	2019/11/15
1.8	Add RecommEnded operating conditions	2020/2/27
1.9	Update format	2021/2/25
2.0	Changed MSL	2021/3/29
2.1	Change Tape and Reel Information of SOW16	2021/5/24
2.2	Corrected NSi8100W MSL to 2	2021/6/28
2.3	Change Storage Temperature, Device Information, VIH2/VIL2, V_{ILT} comments, Part number. Delete NSi8101. Update Insulation and Safety Related Specifications, add Junction Temperature, update Insulation and Safety Related Specifications part, add Safety-Limiting Values part	2022/9/7

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