NSM3011/NSM3012/NSM3013

Hall-Effect Based Angle Sensor IC with Common-Mode Field Rejection

Datasheet (EN) 1.0

Product Overview

NSM301X is a contactless angle sensor that provides high-accuracy angle position measurement with wide temperature range from -40℃ to 125℃.

NSM301X senses the magnetic field strength which is generated by the two-pole magnet based on an integrated Hall element array and converts the magnetic field strength into angular position of the magnet through the internal DSP. NSM301X provides different outputs include analog voltage, PWM, OWI, SPI, UVW.

The NSM301x provides SPI and OWI interfaces for signal path configuration. The output characteristics of NSM301x can be configured according to users' requirement (such as output interface, gain, clamping values, output filter, etc.).

The chip supports 3.3V, 5V power supply voltage (different power supply versions).

Key Features

- 14-bit Analog output DAC/ 12-bit PWM output
- The internal automatic gain compensation circuit can compensate for the gain loss caused by the temperature characteristics and the installation position tolerance in the Z direction of the magnet.
- Support four segment linear fitting
- ±0.2° accuracy after four-segment calibration
- SON digital output to judge the strength of magnetic field with programmable threshold
- Abnormal diagnosis function
- Differential Hall sensor for stray field suppression
- SPI and OWI programmable interface
- NOVOSENSE innovative 'Spin Current' technology for offset temperature drift suppression
- Operating temperature: -40℃ ~ 125℃
- AEC-Q100 reliability standard: Grade 1
- RoHS & REACH Compliant
- Lead-free component, suitable for lead free soldering profile:260℃, MSL3

Applications

- Rotary angle position measurement
- Valve rotation angle measurement
- Accelerator pedal angle sensor
- Contactless rotary switch button
- Replace the traditional knob type sliding rheostat
- Home printer
- Hand-held marking machine
- Industrial steering gear angle sensor

Device Information

Part Number	*Package*	*Power Supply*	*Version*
NSM3011A-DSPR	SOP8	5V	Industrial
NSM3011A-Q1SPR	SOP8	5V	Auto
NSM3012A-DSPR	SOP8	5V	Industrial
NSM3012A-Q1SPR	SOP8	5V	Auto
NSM3013A-DSPR	SOP8	5V	Industrial
NSM3013A-Q1SPR	SOP8	5V	Auto
NSM3011B-DSPR	SOP8	3.3V	Industrial
NSM3011B-Q1SPR	SOP8	3.3V	Auto
NSM3012B-DSPR	SOP8	3.3V	Industrial
NSM3012B-Q1SPR	SOP8	3.3V	Auto

NSM3013B-DSPR	SOP8	3.3V	Industrial
NSM3013B-Q1SPR	SOP8	3.3V	Auto

	NSM3011	*NSM3012*	*NSM3013*
OWI	√	√	√
SPI	×	√	×
Analog Output	√	√	√
PWM Output	√	√	√
UVW Output	×	×	√
SON	×	×	√

Functional Block Diagrams

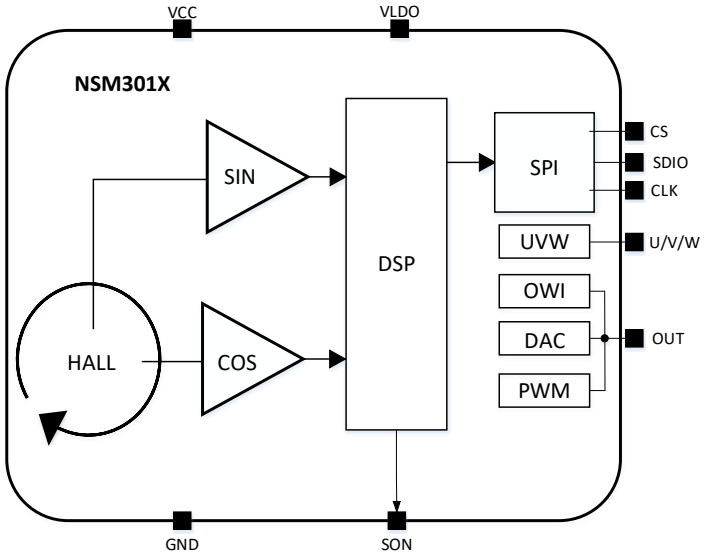

Figure 1 NSM301x Block Diagram

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1. Pin Configuration and Functions

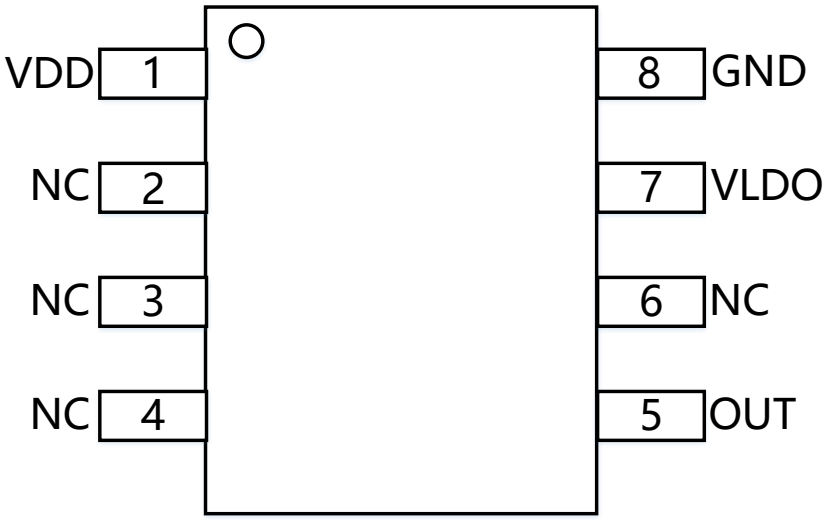


Figure 1.1 NSM3011 Package

Table 1.1 NSM3011 Pin Configuration and Description

NSM3011 PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD	Power supply
2	NC	No connection (Connect to GND for optimal ESD performance)
3	NC	No connection (Connect to GND for optimal ESD performance)
4	NC	No connection (Connect to GND for optimal ESD performance)
5	OUT	Analog output/ PWM output / OWI
6	NC	No connection (Connect to GND for optimal ESD performance)
7	VLDO	Internal LDO output
8	GND	Ground

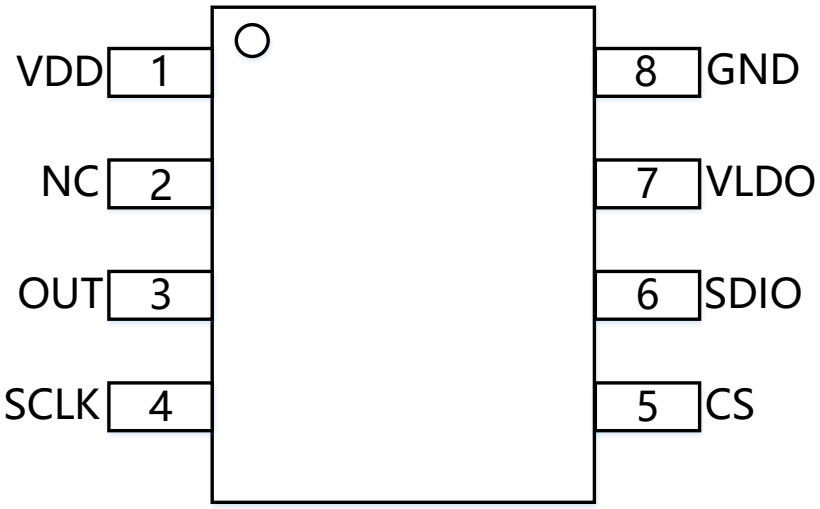


Figure 1.2 NSM3012 Package

Table 1.2 NSM3012 Pin Configuration and Description

NSM3012 PIN NO.	***SYMBOL***	***FUNCTION***
1	VDD	Power supply
2	NC	Not connection
3	OUT	Analog output/PWM output/OWI
4	SCLK	3-wires SPI SCLK
5	CS	3-wires SPI CS
6	SDIO	3-wires SPI SDIO
7	VLDO	Internal LDO output
8	GND	Ground

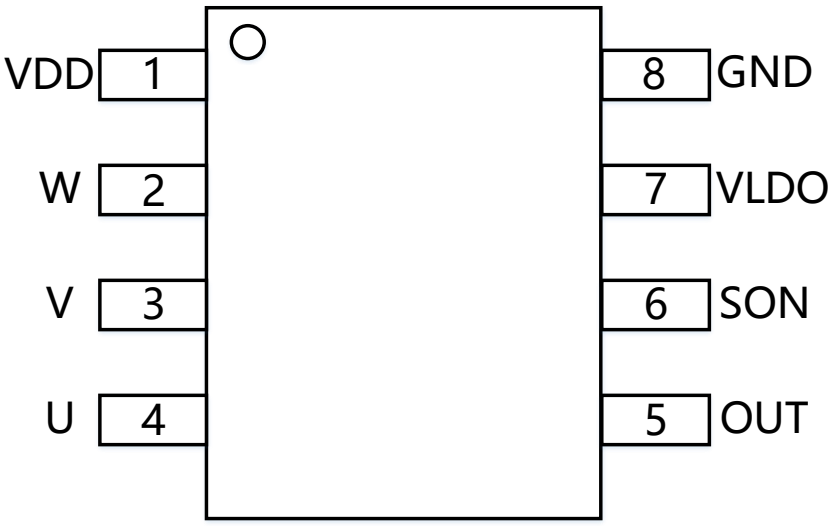


Figure 1.3 NSM3013 Package

Table 1.3 NSM3013 Pin Configuration and Description

NSM3013 PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD	Power supply
2	W	W output
3	V	V output
4	U	U output
5	OUT	Analog output/PWM output/OWI
6	SON	SON output
7	VLDO	Internal LDO output
8	GND	Ground

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Voltage	VDD	-0.3		6.5	V	@25℃
Output voltage		-0.3		VDD+0.3	V	@25℃
Output current	Iout	-15		15	mA	
Storage temperature	$T_{Storage}$	-40		150	℃	
Ambient temperature	$T_{operation}$	-40		125	℃	
Lead temperature	T_{lead}		260		℃	
ESD			±4		kV	HBM
			±0.5		kV	CDM

3. Specifications

(TA= -40°C to 125°C, VCC = 5V, unless otherwise specified)

3.1. Power Supply

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Nominal Supply Voltage [1]	VDD	3	3.3	5.5	V	3.3V Verison
		4.5	5	5.5	V	5.0V Verison
Supply current	Isy	7.5	10	12.8	mA	5.0V Verison
Power-On reset time[1]	ton		3		ms	Disable OWI & AGC@25℃
Power-On reset (rising) [1]	POR_LH		2.78		V	3.3V @25℃
			2.9		V	5.0V @25℃
Output short current[1]	I_Short		15		mA	5.0V Verison

3.2. Analog Output Characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Linear range of proportional output [1][2]	Vout	5%		95%	VDD	
Low abnormal diagnosis [1][2]	Vdiag_L			3%	VDD	RL >= 10 kΩ@25℃
High abnormal diagnosis [1][2]	Vdiag_H	97%			VDD	RL >= 10 kΩ@25℃
DAC Resolution[1]			14		Bit	@25℃
DAC INL[1][2]	INL		±3		LSB	@25℃
DAC DNL[1][2]	DNL		±1		LSB	@25℃
DAC output noise[1][2]	Vn(rms)		90		uV	Bandwidth 3Khz @25℃
Output slew rate[1][2]	OUT_SR		60		V/ms	Cout<=10nF @25℃
Output load[1]	R_{LOAD}		10		KOhm	Pull up to 5V or pull down@25℃
	C_{LOAD}			100	nF	
Proportional output error[1][2]	Erm	-0.22		0.15	%VDD	

3.3. PWM Output Characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
PWM output interface			Push-Pull			OD/Push-Pull optional

PWM output frequency	fpwm	970	1000	1030	Hz	11 Bit Effective Resolution
		475	500	525	Hz	12 Bit Effective Resolution
		242.5	250	257.5	Hz	13 Bit Effective Resolution
		97	100	103	Hz	14 Bit Effective Resolution
PWM resolution[1]			12		Bit	
PWM low logic level	PWM_VL			0.35	V	I_{Load} <=4mA
PWM high logic level	PWM_VH	VDD-0.35			V	I_{Load} <=4mA
Low abnormal diagnosis [1][2]	PWM_Diag_L	0			%	AGC=0 & PWM_DIAG=1
High abnormal diagnosis[1][2]	PWM_Diag_H			100	%	AGC=255 & PWM_DIAG=1
OD mode rise time	PWM_ODRT		20	25.6	us	C_L=10nF, R_L=1 KΩ
OD mode fall time	PWM_ODFT		4	7	us	C_L=10nF, R_L=1 KΩ
Push-pull mode rise time	PWM_PPRT		4	7	us	C_L=10nF, R_L=1 KΩ
Push-pull mode fall time	PWM_PPFT		4	7	us	C_L=10nF, R_L=1 KΩ
PWM Jitter	J_{PWM}		±0.04	±0.225	Hz	C_L=10nF, R_L=1KΩ,500Hz
			±0.04	±0.15	Hz	C_L=10nF, R_L=1 KΩ,250Hz
			±0.04	±0.15	Hz	C_L=10nF, R_L=1 KΩ,100Hz
			±0.04	±0.45	Hz	C_L=10nF, R_L=1 KΩ,1000Hz

3.4. IO Characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
High logic level input[1]	V_IH	0.7*VDD		VDD	V	
Low logic level input[1]	V_IL	0		0.3*VDD	V	
Leakage current	I_LEAK	-1		1	uA	
High logic level output	V_OH	VDD-0.35			V	I_{Load} <= 4mA
Low logic level output	V_OL			VSS+0.35	V	$_{ILoad}$ <=4mA
SDO rise time	MISO_RT		35	60	ns	C_L = 30 pF, R_L = 10 kΩ
SDO fall time	MISO_FT		35	60	ns	C_L = 30 pF, R_L = 10 kΩ
SPI communication rate[1][2]				10	MHz	
OWI communication rate[1][2]				50	KHz	

3.5. Magnetic Characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Magnetic field strength		20		80	mT	Internal Measurement Value at Z Direction
Diameter			6		mm	
Thickness			2.5		mm	
Pitch between Magnet and Chip		0.5		3	mm	
Allowable tolerance of center in XY direction		0.3		0.3	mm	
Magnetic field strength			NdFeB35			

3.6. UVW Output Characteristics

UVW Output Characteristics						
Supported number of pole pairs[1]	UVW_PP	1		8	PP	Pole pairs
High logic level output	UVW_OH	VDD-0.35			V	I_{Load}<=4mA
Low logic level output	UVW_OL			0.35	V	I_{Load}<=4mA
UVW output hysteresis[1]	UVW_Hys	1		4	LSB	

3.7. System Characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Angle Accuracy		-1.0		1.0	°	6mm*2.5mm UMAG magnet & Eccentricity error=±0.3mm & Pitch between Magnet and Chip=2mm
System Delay[1]	Tdelay		120		us	Without dynamic angle compensation
			10		us	With dynamic angle compensation

[1]: Guaranteed by design

[2]: Guaranteed by minichar experiment & verification

4. Function Description

4.1. Overview

NSM301X is a high-integrated hall-effect-based rotary angle sensor IC. The sensor IC is mainly used in angle measurement filed such as motor rotation. NSM301X integrates a planar Hall sensor to sense the magnetic field component in Z direction and converts the magnetic strength into voltage. The voltage signal from the Hall sensor will be conditioned and converted by an analog to digital converter (ADC). The output of the ADC is processed by the CORDIC algorithm module of the DSP to calculate the angle and magnitude of the magnetic field. The internal automatic gain control (AGC) of IC can compensate for the change in temperature and magnetic field. NSM301X provides different outputs include analog voltage, PWM, OWI, SPI, UVW. NSM301x has the internal Multi-Time Programmable memory (MTP) and it can be programmed through the industry standard SPI and OWI interface. NSM301x supports programmable zero angle (start position) and the maximum angle (end position), and map the output to the full angle range from 0° to 360°. Figure 4.1 is the block diagram of NSM301x.

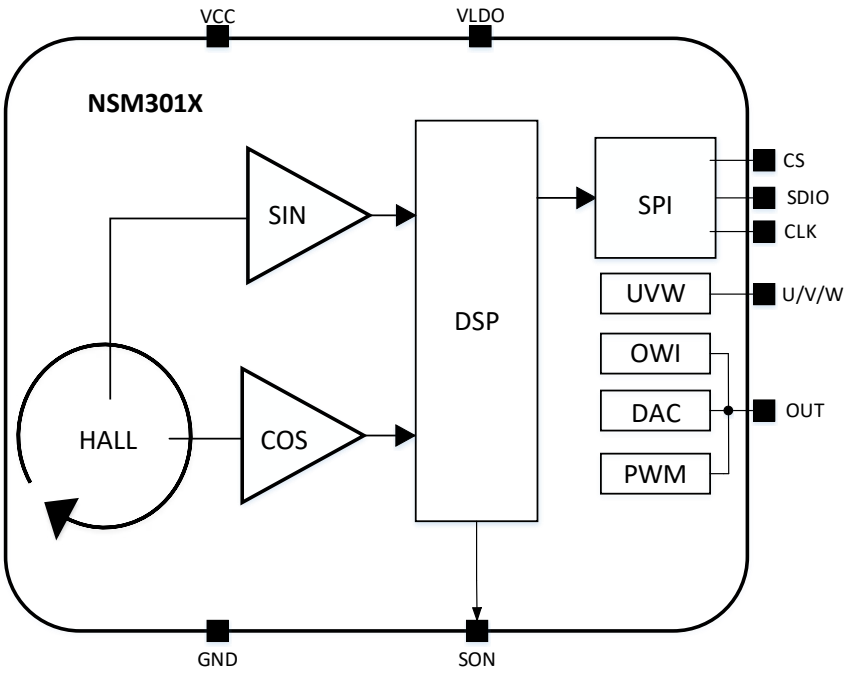


Figure 4.1 Block Diagram

4.2. Power Management

NSM301xA is 5V power supply version and NSM301xB is a 3.3V power supply version. For 5V version, VLDO output is 4V. MTP can be programmed and erased. For 3.3V power supply version, the output voltage of VLDO is 3.3V. The MTP of this version is read-only, so users cannot program.

4.3. Analog Output

The default output mode of NSM301x is analog linear output. The characteristics are as follows:

- The full-scale reference voltage of the output is the power supply voltage, and the change of the output voltage will be proportional to the change of the power supply voltage.
- The angle value measured by sensor determines the ratio of output voltage to power supply voltage.

- Users can redefine the linear correspondence between the output voltage and the angle by reconfiguring the four-segment compensation register.
- Users can configure the value of the clamp register to constraint the output voltage to a specified range.
- NSM301X provides abnormal diagnosis function. User can activate this function through configuration. When the NSM301x detects an abnormal state, the VOUT voltage will exceed the normal linear output range. The HIGH diagnosis output voltage is not lower than 97% of VDD, and the LOW diagnosis voltage of VOUT is not higher than 3% of VDD.

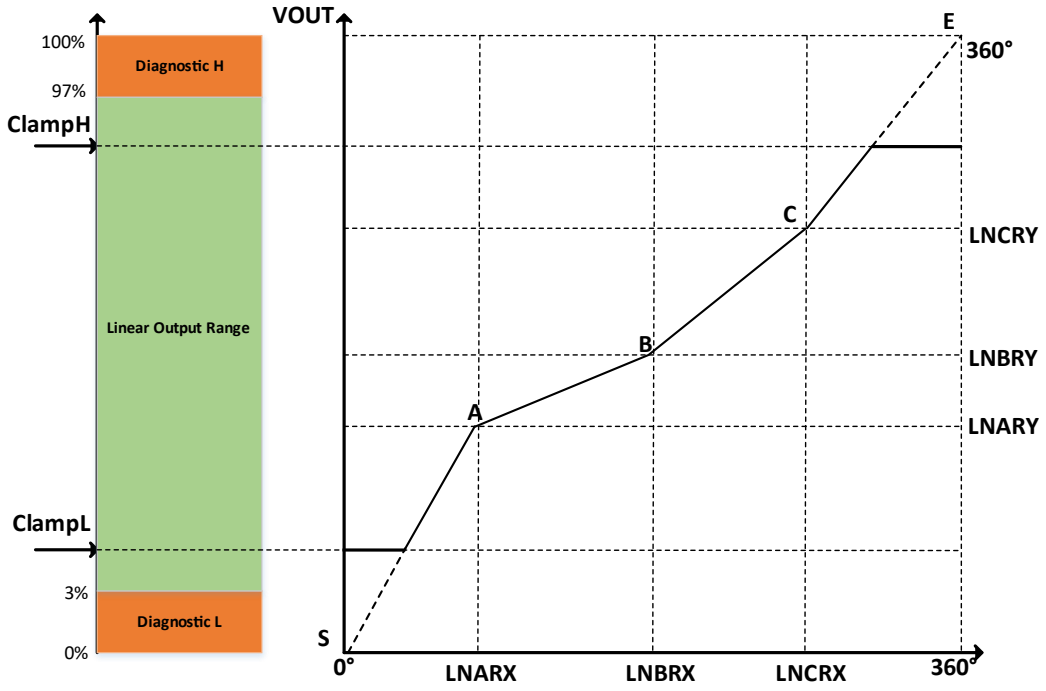


Figure 4.2 Analog output function

The figure above is a typical transfer function curve after users' configuration.

- The configuration values of VClampH and VClampL determine the maximum and minimum output values of Vout (corresponding to % of VDD).
- The value of LNRA/B/C determined the three turning points of four-segment fitting linear function.
  - When the measurement angle θ <= LNRAX, the transfer function is a straight line formed by 0° (0%) and LNRAX (LNRAY).
  - When measuring the angle LNRAX<θ<=LNRBX, the transfer function is a straight line formed by LNRAX (LNRAY) and LNRBX (LNRBY).
  - When measuring the angle LNRBX<θ<= LNRCX, the transfer function is a straight line formed by LNRBX (LNRBY) and LNRCX (LNRCY).
  - When measuring the angle θ> LNRCX, the transfer function is a straight line formed by LNRCX (LNRCY) and 360°(100%).
  - The limit of set value is:
    - 0 <= LNRAX <= LNRBX <= LNRCX <= 16383
    - 0<= LNRAY/BY/CY <= 16383

- The corresponding output of the start and end points of the transfer function fitted by the 4-segment method is 0V and VDD voltage by default. Users can change the start and end points through programming. The start point position depends on the slope of the first segment which can be configured by the LNR_SAK register and the point A which can be configured by LNRAX and LNRAY register. The end point position depends on the slope of the 4th segment which can be configured by the LNR_CEK register and the point C which can be configured by LNRCX and LNRCY register.

4.4. PWM Output

The PWM output can be configured as push-pull and open drain modes, as shown in the figure below. Users can configure the interface according to the application. The characteristics of PWM output are as follows:

- The angle value measured by NSM301x determines the duty cycle of the PWM output signal. Without any configuration by the user, the angle from 0° to 360° corresponds to the PWM output duty cycle from 10% to 90%.
- Users can redefine the linear correspondence between output PWM duty cycle and angle value by reconfiguring registers.
- Users can set the value of the clamp register to limit the output duty cycle to a specified range.
- NSM301X provides abnormal diagnosis function. User can activate this function through configuration. When the NSM301x detects an abnormal state, the PWM output will be the specific duty cycle (0% or 100%).

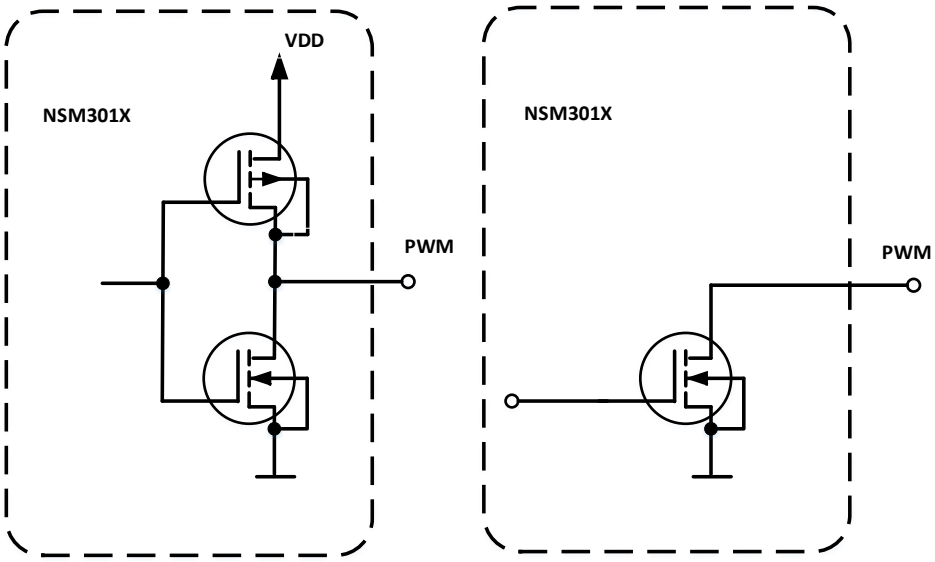


Figure 4.3 PWM Output IO

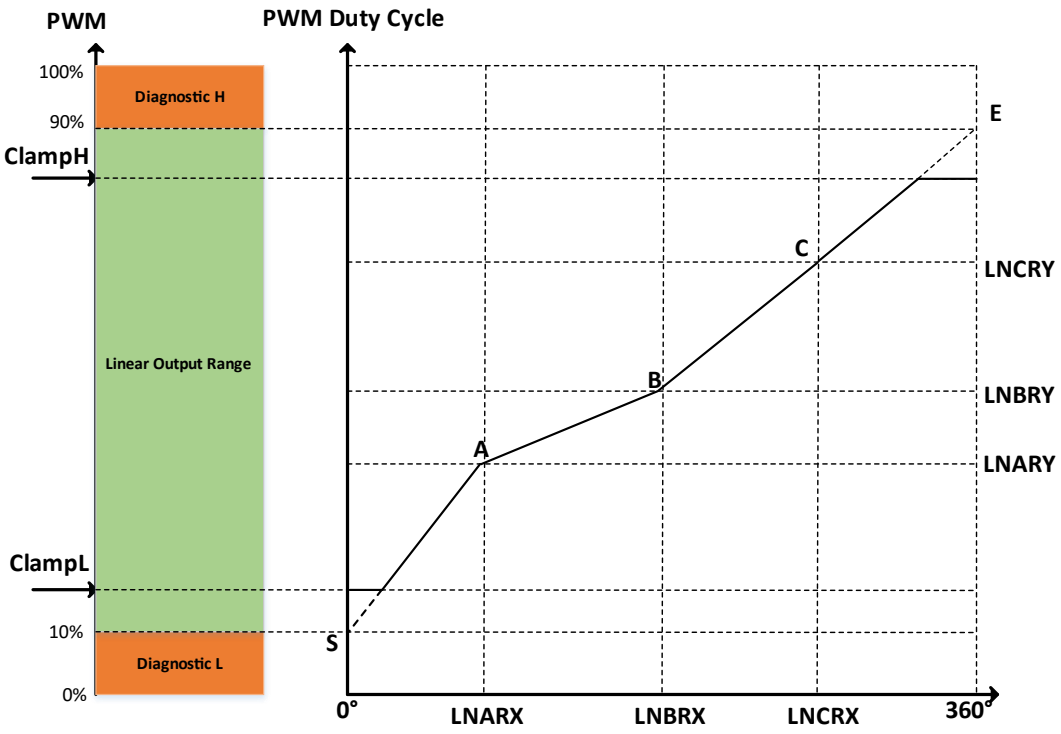


Figure 4.4 PWM output function

The figure above is a typical transfer function curve after users' configuration.

- The configuration values of VClampH and VClampL determine the maximum and minimum output values of Vout (corresponding to % of VDD).
- The value of LNRA/B/C determined the three turning points of four-segment fitting linear function.
  - When the measurement angle θ <= LNRAX, the transfer function is a straight line formed by 0° (0%) and LNRAX (LNRAY). (There is a special case that when the value of LNRAX is set to 0, the output duty cycle of the PWM corresponding to 0° will no longer be equal to 10%, but is determined by the set value of LNRAY).
  - When measuring the angle LNRAX<θ<=LNRBX, the transfer function is a straight line formed by LNRAX (LNRAY) and LNRBX (LNRBY).
  - When measuring the angle LNRBX<θ<= LNRCX, the transfer function is a straight line formed by LNRBX (LNRBY) and LNRCX (LNRCY).
  - When measuring the angle θ> LNRCX, the transfer function is a straight line formed by LNRCX (LNRCY) and 360° (100%). (There is a special case that when the value of LNRCX is set to 16383, the output duty cycle of the PWM corresponding to 360° will no longer be equal to 90%, but is determined by the set value of LNRCY).
  - The limit of set value is:
    - 0 <= LNRAX <= LNRBX <= LNRCX <= 16383
    - 0<= LNRAY/BY/CY <= 16383

4.5. Direction Setting

The direction of angle increment is determined by the setting value of the DIR bit in the Config1 register. When the value of DIR is 0, the direction of angle increase is clockwise. When the value of DIR is set to 1, the direction of angle increase is counterclockwise.

4.6. AGC Setting

The NSM301x has an automatic gain (AGC) adjustment module. The NSM301x can adjust the gain of the signal path according to the strength of the sensed magnetic field. The input signal is amplified to occupy the most range of NSM301x internal ADC, thereby improving sampling accuracy. This can ensure that the NSM301x adapt to different mechanical constraints and magnetic fields.

The default gain of signal chain is 16 times. Users can change the fixed gain by configuring the AGC_FIX register. The user can also enable the AGC function by configuring the CONFIG2 register. After the AGC function is enabled, the fixed gain configured by the AGC_FIX register will be invalid. If the user uses the SON function of the NSM3013, the AGC function needs to be disabled. In other scenarios, the user can choose to enable the AGC function.

4.7. Zero Position Setting

User can configure ZERO_POSITION register to match the mechanical angle and electrical angle. The user can turn the mechanical angle to zero position and write the corresponding measured angle value into the ZERO_POSITION register. This setting can align the mechanical reference zero angle position with the electrical reference zero angle position.

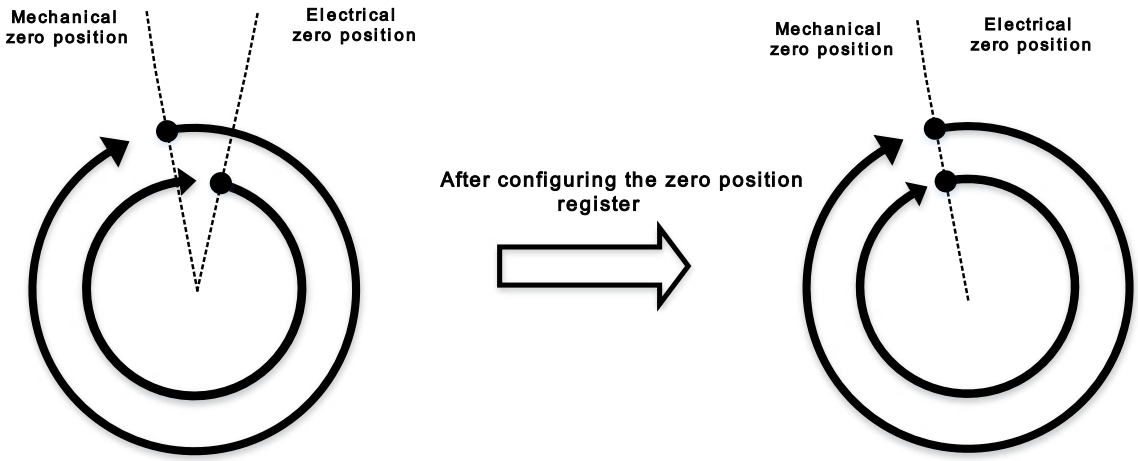


Figure 4.5 Zero position setting

4.8. SON Setting

The NSM301X senses the magnetic field strength in Z direction. SON digital output can judge the strength of magnetic field with programmable threshold. The magnetic field strength can reflect the gap between the magnet and the IC in the Z direction in most applications.

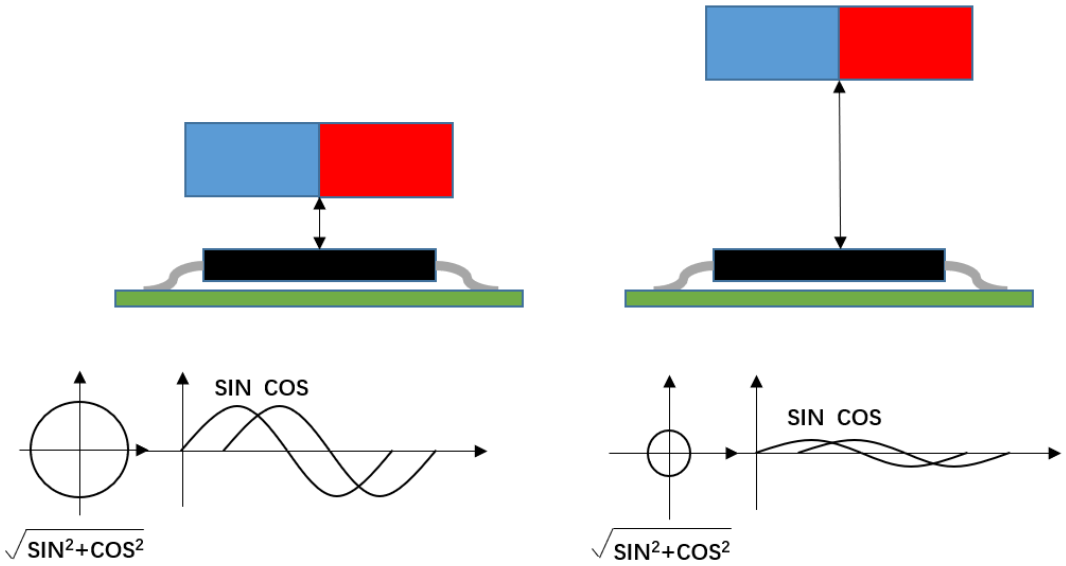


Figure 4.6 SON function

NSM3013 provide SON function. SON function is used to determine the pitch between the magnet and the IC in the Z direction. The principle of SON is hysteresis comparison. Users can set high/low threshold value by setting MAG_THRES_HIGH & MAG_THRES_LOW register. When the user's SON_POL is set to 0, when the magnetic strength SIN2+COS2 is greater than the setting value of MAG_THRES_HIGH, the SON pin will become high output, and when it is less than the setting value of MAG_THRES_LOW, the SON pin will become low output. If SON_POL is set to 1, the logic of the SON pin will be reversed.

4.9. Output Data Rate

NSM301X have 8 different output rate mode. When the OUTFILTER is configured to 0, the angle output rate is 31.25KHz. If the OUTFILTER is configured from 1 to 7, the angle output response speed will operate from 1/2 to 1/128 of the original rate.

4.10. UVW Output

The output mode of UVW interface is push-pull output, as shown in the figure below. NSM3013 support UVW output mode. When the chip is powered on, the UVW three-phase output is low logic. UVW output starts after the end of the first calculation cycle. NSM3013 supports programmable pole-pair output up to 8 pairs. The figure below shows the case when the number of pole-pairs is 1.

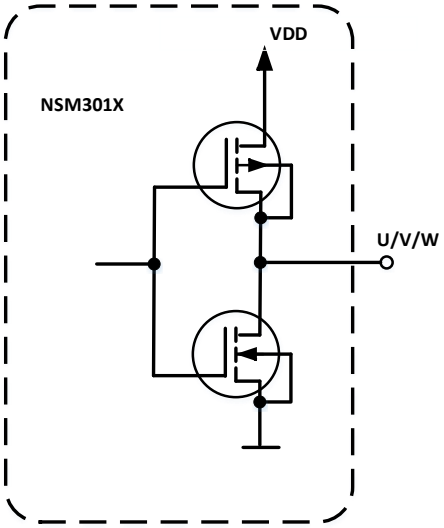


Figure 4.7 UVW IO

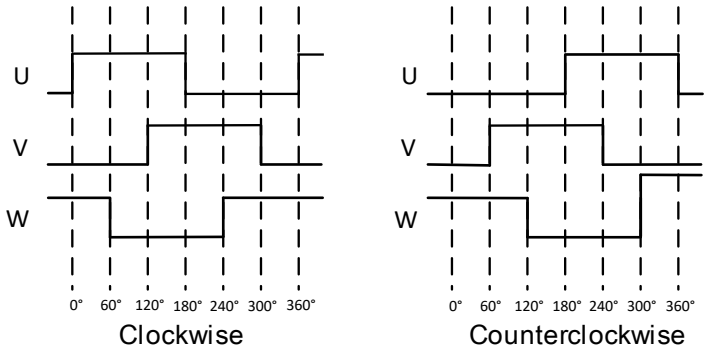


Figure 4.8 UVW output signal

4.11. SPI Communication

NSM3012 supports three-wire SPI interface consists of three signals: CS, SDIO, SCK. CS pin is used to activate SPI communication. When CS is High， the SDIO pin is in a high-impedance state. CS is pulled high by default. CS should be low before data transactions and must stay at low level for the entire SPI communication period. The communication sequence is shown in the

following figure:

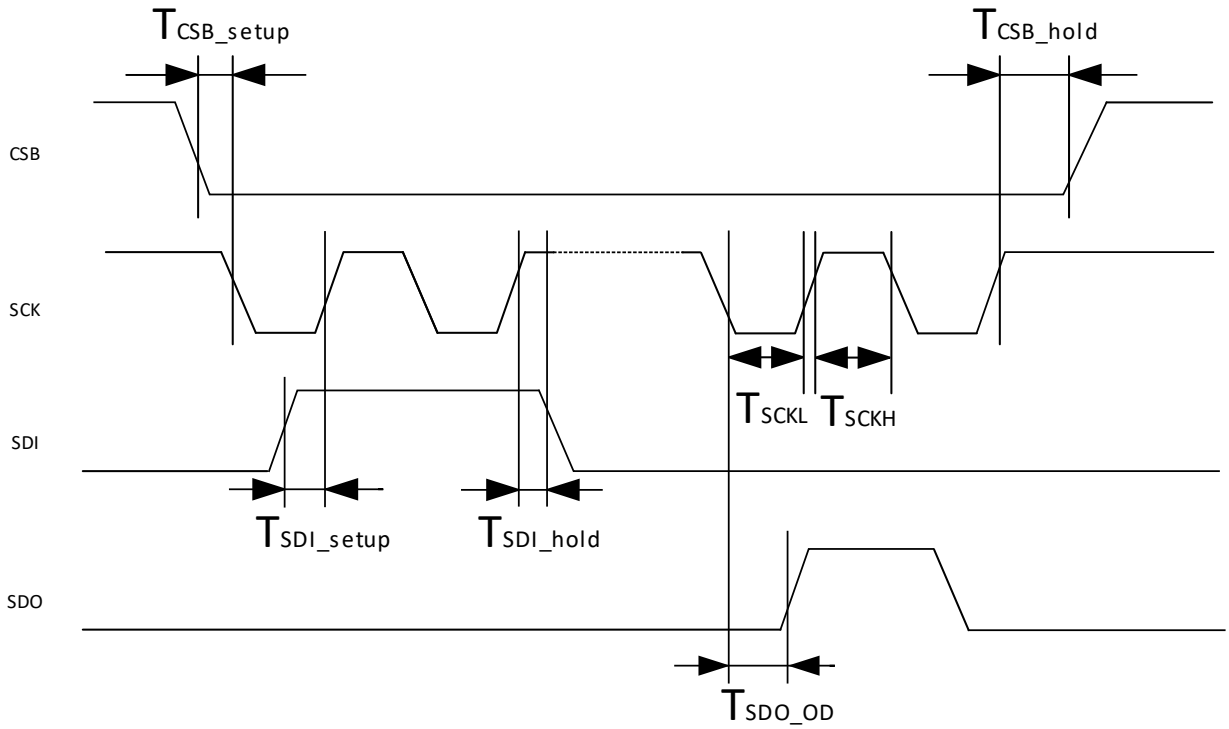


Figure 4.9 SPI Communication timing

Symbol	*Parameter*	*Comments*	*Min*	*Typ*	*Max*	*Unit*
t_{CSB_setup}	CSB falling edge to SCK falling edge		250	-	-	ns
t_{CSB_hold}	SCK last rising edge and CSB rising edge		250	-	-	ns
t_{SCKL}	Low period of clock		250	-	-	ns
t_{SCLH}	High period of clock		250	-	-	ns
t_{SDI_setup}	Setup time of SDI data		40		-	ns
t_{SDI_hold}	Hold time of SDI data		40	-	-	ns
t_{SDO_OD}	Data valid time of SDO		-	-	40	ns

When CSB is low level, the first rising edge of SCLK marks the beginning of the SPI transfer. The 16-bit instruction bits are transmitted first, followed by configurable 1/2/3 or more bytes of data. As shown in the figure, the 16-bit instruction bit is divided into the following parts.

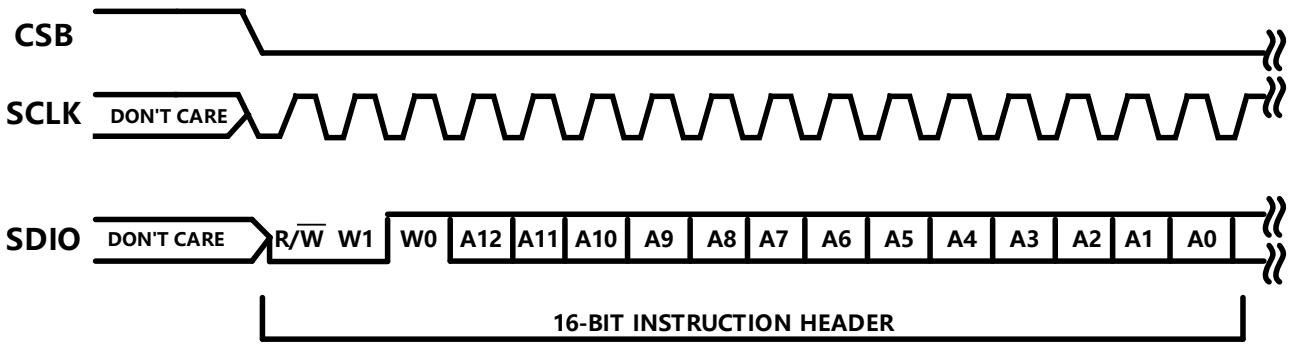


Figure 4.10 SPI output command

The highest bit of the data stream is the read/write bit. A high level indicates a read operation, and a low level indicates a write operation. W1 and W0 command represent the number of bytes to read or write.

If the number of bytes is less than 3 (W1 & W2 command: 00, 01, or 10), CSB can be temporarily pulled high between every bytes of data transmission. After CSB is pulled low again, data transmission will continue.

If W1/W0 is set to 11, the number of bytes is unlimited and can be transmitted sequentially until the CSB is pulled high. The CSB is not allowed to be pulled high temporarily between the transmitted bytes.

The bits A12-A0 specify the register address for reading and writing. If more than one byte of data is transmitted, the data will be transmitted to subsequent addresses.

The settings of W1 and W0 are shown in the following table:

W1:W0	*Function*	*CSB temporarily pulled high*
00	1 byte data transmission	Optional
01	2 bytes data transmission	Optional
10	3 bytes data transmission	Optional
11	More than 4 bytes data transmission. CSB keep low logic.	Forbidden

The 16-bit instruction header is followed by data bytes. The length of the data is determined by the W0 and W1 bits, which can be more than one byte.

Data transmission sequence is selected by the ‘LSB_first’ bit. After the chip is powered on, the default is high bit priority, which can be changed through the configuration register. In the high bit first mode, the transmission starts from the highest bit to the lowest bit. In the low bit first mode, the transmission sequence is from LSB to MSB。

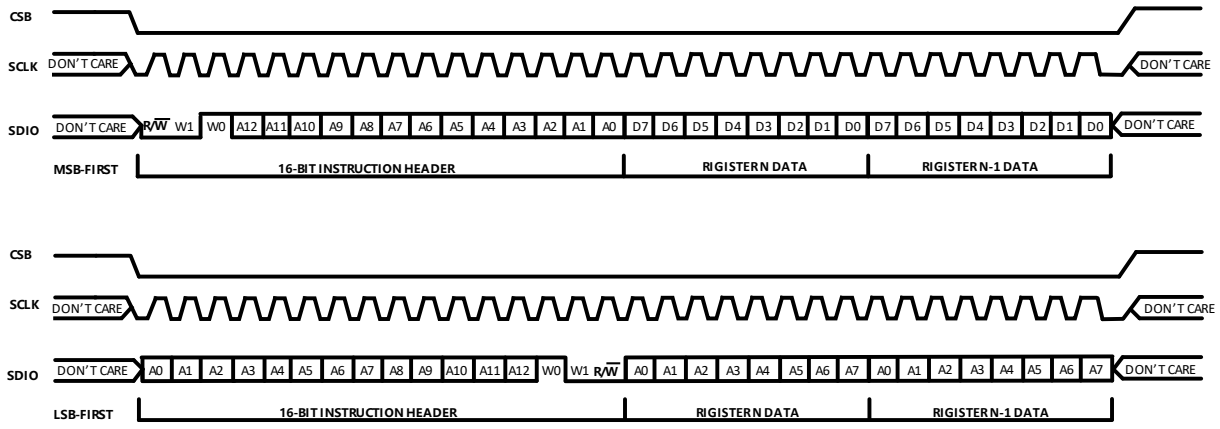


Figure 4.11 SPI command in MSB-FIRST mode and LSB-FIRST mode

4.12. OWI Communication

OWI interface mode can be activated within the 20ms period after the end of the internal POR by inputting a 24-bit specific OWI entry command (0xB5A6FF) through the OWI pin in this window and the analog output will be disabled. If OWI entry command is not detected within the 20ms window, the chip will operate in analog output mode. Writing 1 to the OWI_Disable bit can permanently disable OWI communication. For NSM3011, it is prohibited to write 1 to the OWI_Disable bit.

The figure below is OWI communication protocol:

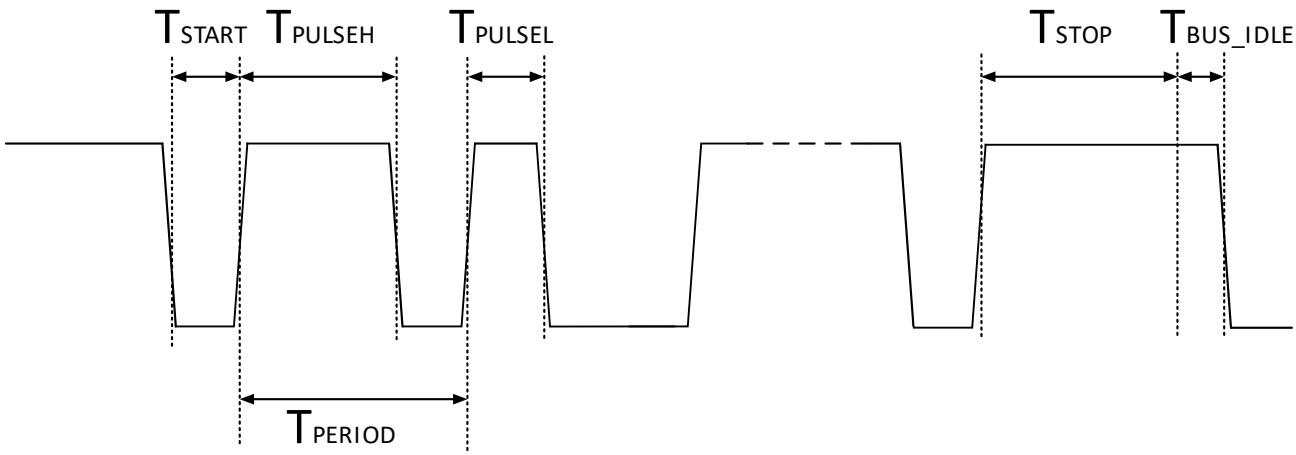


Figure 4.12 OWI Timing

Signal	Parameter	Comments	Min	Typ	Max	Unit
t_{Period}	OWI Time Slot		20		1000	us
t_{Period_DEV}	OWI Time Slot deviation		0.75	1	1.25	t_{Period}
t_{PulseL}	W/R 0 low time		1/8	1/4	3/8	t_{Period}
t_{PulseH}	W/R 1 low time		5/8	3/4	7/8	t_{Period}
t_{Start}	Time for transmission start		10			us
t_{Stop}	Time for transmission stop	2 numbers of t_{Period}	2			t_{Period}
				4		ms
t_{Bus_Idle}	Idle time	The recovery time between each bit transmission	10			us

The OWI entry command is shown in the figure:

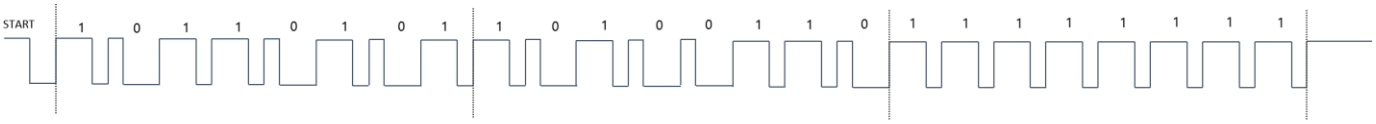


Figure 4.13 OWI entry command

In OWI mode, the bit period (tperiod) is determined by the last bit period of the OWI entry command and cannot be changed during OWI communication process.

The OWI bus protocol is defined as follows:

a) Idle state:

If there is no communication between host and sensor, the OWI bus is in an idle state. In this state, the OWI pin is in the input state and is pulled up to a high level by an external pull-up resistor.

b) Start conditions:

When the OWI bus is in the idle state, the host sends a low-level pulse (20us-4ms) to mark the beginning of an OWI communication.

c) End conditions:

If all data has been written or read, the OWI communication will automatically end, and the OWI bus will return to the idle state.

If the OWI bus maintains a fixed high or low level for more than twice tperiod, the OWI communication will be forcibly ended, and the OWI bus will return to the idle state.

d) Addressing and R/W control:

The OWI host needs to send addressing and read/write control information after sending the start condition, including 8-bit register address (MSB first), 2-bit byte number control bit and 1-bit read-write control bit. The byte number control bit indicates the number of bytes read/write. (00: read/write 1 byte, 01: read/write 2 bytes, 10: read/write 3 bytes, 11: read/write 4 bytes) The read and write control bit indicates read operation or write operation (0: write operation, 1: read operation).

e) Write operation

The OWI host sends the write control bits to activate write operation mode. The host will continue to send 1/2/3/4 bytes (determined by the number of bytes control bits), and the data will be sequentially written to the specified register address and subsequent address, as shown in Figure below.

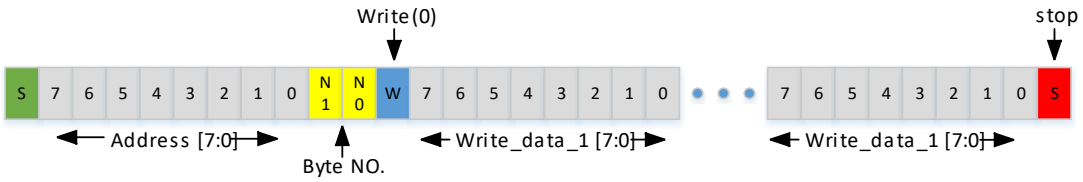


Figure 4.14 OWI write

f) Read operation:

After the OWI host sends the read and write control bits, the chip will start to send the data of the 1/2/3/4 (determined by the number of bytes control bit) byte of the specified register address and 2-bit parity check code (C1 and C0). The OWI host regains control of the bus after receiving all the data. As shown in Figure 5.5.

C1 = Read_data[7] ^ Read_data[5] ^ Read_data[3] ^ Read_data[1];

C0 = Read_data[6] ^ Read_data[4] ^ Read_data[2] ^ Read_data[0].

The OWI host can judge whether the read data is correct according to the parity bit.

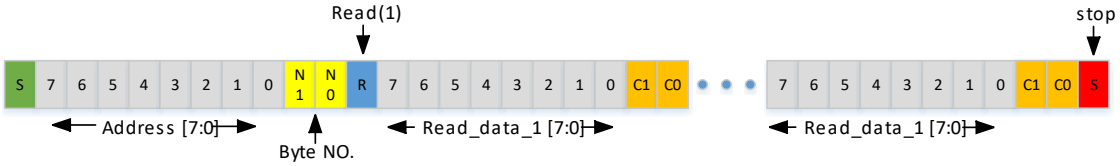


Figure 4.15 OWI read

5. Register Map

Address	*R/W*	*Register Name*	*Function*	*Default Value*
0x00	RW	SPI Config	BIT<7,0>: SDO_ACTIVE BIT<6,1>: LSB First BIT<5,2>: Soft Reset SDO_ACTIVE: 0 SPI Active LSB_FIRST: 1 LSB First， 0 MSB First SoftReset: 1	0x00
0x03	R	AGC_GAIN	1~254: Gain Value， 0 & 255: AGC WARNING	0x01
0x04	R	MAGH	MAGNITUDE High 6 Bit	0x00
0x05	R	MAGL	MAGNITUDE Low 8 Bit	0x00
0x06	R	ANGLEH	ANGLE High 6 Bit	0x00
0x07	R	ANGLEL	ANGLE Low 8 Bit	0x00
0x08	R	CRC	CRC Value of ANGLE Register	0x00
0x09	R	STATUS	BIT<7>: Data_RY: Angle Data Ready BIT<4>: ABZ_Overspeed BIT<3>: ADC_Overflow_cos: COS Overflow BIT<2>: ADC_Overflow_sin: SIN Overflow BIT<1>: AGC_WARNING_H: AGC High Gain Warning BIT<0>: AGC_WARNING_L: AGC Low Gain Warning	0x00
0x10	RWB	CONFIG1	BIT<7>: owi_dis: Disable OWI BIT<6>: hsy_en: 1, Enable angle hysteresis BIT<5,4>: filter_step 00-Close POST FILTER, 01-POST FILTER 1, 10-POST FILTER 2 11-POST FILTER 3 BIT<3>: 4-seg_dis: Disable four segment compensation BIT<2>: 4-seg_polarity:	0x00

			0: Positive slope SAk/ABk/BCk/CEk, 1: Negative slope SAk/ABk/BCk/CEk BIT<1>: DIR: 0--Clockwise, 1--Counterclockwise BIT<0>: out_mode: 0-Analogoutput, 1--PWM output	
0x11	RWB	CONFIG2	BIT<7>: son_pol: son polar BIT<6>: AGC_dis 1: disable AGC BIT<5>: AGC_Target 0： range of 80%ADC 1： range of ADC BIT<4:2>: OUTFILTER 000--1 time average of angle output result 001--2 time average of angle output result 010--3 time average of angle output result ⋮ 111--128 time average of angle output result BIT<1:0>: DEAC 00-disable dynamic angle compensation 01-1st order dynamic angle compensation It is forbidden to configure 01 and 11 for user	0x00
0x13	RWB	PWM_UVW_CONF	BIT<0>: PWM_MODE 0：push pull，1：OD BIT<2:1>: PWM_RANGE Set PWM output Range。00：10%~90%， 01：5%~95%，10：0%~100% BIT<4:3>: PWM_RES Set PWM output resolution and frequency 00: RES(12) 500 Hz, 01: RES(13) 250 Hz, 10: RES(14) 100 Hz,11: RES(11) 1000 Hz BIT<7:5>UVWPP Set the number of UVW pole pairs，1~8pp	0x00
0X14	RWB	AGC_FIX	Set AGC fixed gain 0~255	0x00
0x15	RWB	DEAC_TDH	Dynamic angle compensation time: High 3 bit	0x00
0x16	RWB	DEAC_TDL	Dynamic angle compensation time: Low 8 bit	0x00
0x17	RWB	CLAMPHH	Four segment compensation ClampH: High 6 bit	0x00
0x18	RWB	CLAMPHL	Four segment compensation ClampH: Low 8 bit	0x00

0x19	RWB	CLAMPLH	Four segment compensation ClampL: High 6 bit	0x00
0x1a	RWB	CLAMPLL	Four segment compensation ClampL: Low 8 bit	0x00
0x1b	RWB	LNR_SAKH	Four segment compensation 1st slope: High 6 bit	0x00
0x1c	RWB	LNR_SAKL	Four segment compensation 1st slope: Low 8 bit	0x00
0x1d	RWB	LNR_ABKH	Four segment compensation 2nd slope: High 6 bit	0x00
0x1e	RWB	LNR_ABKL	Four segment compensation 2nd slope: Low 8 bit	0x00
0x1f	RWB	LNR_BCKH	Four segment compensation 3rd slope: High 6 bit	0x00
0x20	RWB	LNR_BCKL	Four segment compensation 3rd slope: Low 8 bit	0x00
0x21	RWB	LNR_CEKH	Four segment compensation 4th slope: High 6 bit	0x00
0x22	RWB	LNR_CEKL	Four segment compensation 4th slope: Low 8 bit	0x00
0x23	RWB	LNRAXH	Four segment compensation A point LNRAX High 6 bit	0x00
0x24	RWB	LNRAXL	Four segment compensation A point LNRAX Low 8 bit	0x00
0x25	RWB	LNRBXH	Four segment compensation B point LNRBX High 6 bit	0x00
0x26	RWB	LNRBXL	Four segment compensation B point LNRBX Low 8 bit	0x00
0x27	RWB	LNRCXH	Four segment compensation A point LNRAX High 6 bit	0x00
0x28	RWB	LNRCXL	Four segment compensation C point LNRCX Low 8 bit	0x00
0x29	RWB	LNRAYH	Four segment compensation A point LNRAY High 6 bit	0x00
0x2a	RWB	LNRAYL	Four segment compensation A point LNRAY Low 8 bit	0x00
0x2b	RWB	LNRBYH	Four segment compensation B point LNRBY High 6 bit	0x00
0x2c	RWB	LNRBYL	Four segment compensation B point LNRBY Low 8 bit	0x00
0x2d	RWB	LNRCYH	Four segment compensation C point LNRCY High 6 位	0x00
0x2e	RWB	LNRCYL	Four segment compensation C point LNRCY Low 8 bit	0x00
0x2f	RWB	ZERO_POSITIONH	ZERO_POSITION High 6 bit	0x00

0x30	RWB	ZERO_POSITIONL	ZERO_POSITION Low 8 bit	0x00
0x31	RWB	MAGHIGH_THRESH	SON Output High magnitude threshold MAG_THRES High 6 bit	0x00
0x32	RWB	MAGHIGH_THRESL	SON Output High magnitude threshold MAG_THRES Low 8 bit	0x00
0x33	RWB	MAGLOW_THRESH	SON Output Low magnitude threshold MAG_THRES High 6 bit	0x00
0x34	RWB	MAGLOW_THRESL	SON Output Low magnitude threshold MAG_THRES Low 8 bit	0x00
0x35	RWB	ERR_CONFIG	BIT<0>AGCH_warn_en: Enable AGC High gain warning BIT<1>AGCH_warn_high: 1 output high, 0 output low BIT<2>AGCL_warn_en: Enable AGC High gain warning BIT<3>AGCL_warn_high: 1 output high, 0 output low BIT<4>ADC_OF_en: Enable ADC overflow warning BIT<5>ADC_OF_high: 1 output high, 0 output low BIT<6>AMP_OF_en: Enable magnetic strength warning BIT<7>AMP_OF_high: 1 output high, 0 output low	0x00
0x36	RWB	CUSTOMER_ID0	BIT<7:0> Configurable User ID0	0x00
0x37	RWB	CUSTOMER_ID1	BIT<7:0> Configurable User ID1	0x00
0x38	RWB	CUSTOMER_ID2	BIT<7:0> Configurable User ID2	0x00
0x61	W	QUIT_OWI	Exit OWI, 0x5d to analog output，0x89 to high impedance output	0x00
0x62	RWB	QUIT_OWI_CNT	BIT<7:0> Set the time to temporarily exit OWI mode, LSB=65ms	0x00
0x6a	RWB	PROG_MTP	PGM: Programme MTP 0x5d ERASE: Erase MTP 0xa6 EV: Erase verification MTP 0x7c PV: Programmed verification MTP 0xd6	0x00

6. Application Note

6.1. Typical Application Circuit

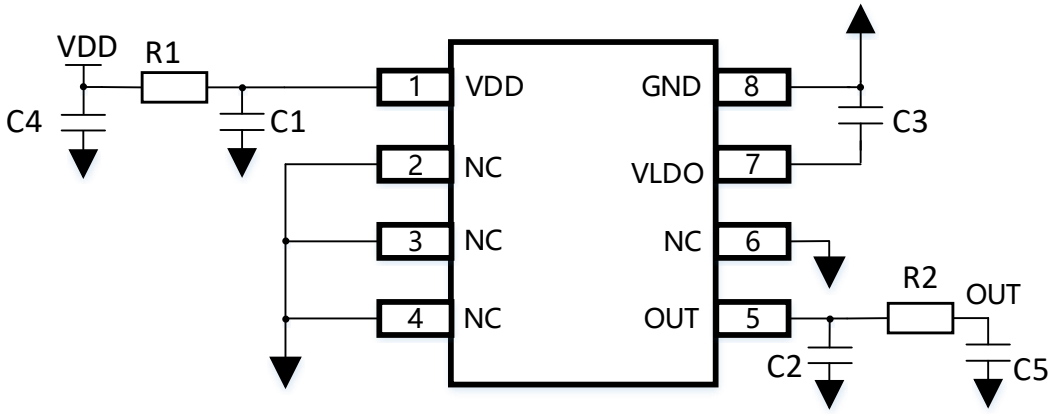


Figure 6.1 NSM3011 Application Circuit

Output	*Compact PCB routing*			*EMC robust PCB routing*			
Analog output	*Min*	*Type.*	*Max*	*Min*	*Type.*	*Max*	*备注*
C_1	100nF	100nF	1uF	47nF	100nF	1uF	
C_2	47nF	100nF	330nF	47nF	100nF	330nF	
C_3	47nF	100nF	220nF	47nF	100nF	220nF	
C_4	-	-	-	500pF	1nF	10nF	
C_5	-	-	-	500pF	1nF	10nF	
R_1	-	-	-	0Ω	10Ω	33Ω	
R_2	-	-	-	10Ω	50Ω	100Ω	

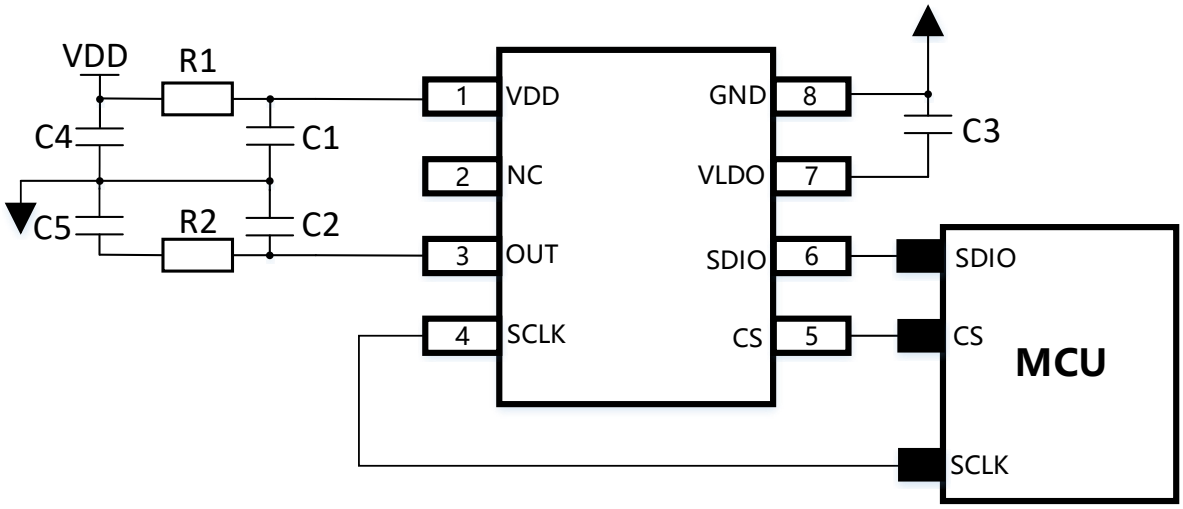


Figure 6.2 NSM3012 Application Circuit

Output	*Compact PCB routing*			*EMC robust PCB routing*			
Analog output	*Min*	*Type.*	*Max*	*Min*	*Type.*	*Max*	*备注*
C_1	100nF	100nF	1uF	47nF	100nF	1uF	
C_2	47nF	100nF	330nF	47nF	100nF	330nF	
C_3	47nF	100nF	220nF	47nF	100nF	220nF	
C_4	-	-	-	500pF	1nF	10nF	
C_5	-	-	-	500pF	1nF	10nF	
R_1	-	-	-	0Ω	10Ω	33Ω	
R_2	-	-	-	10Ω	50Ω	100Ω	

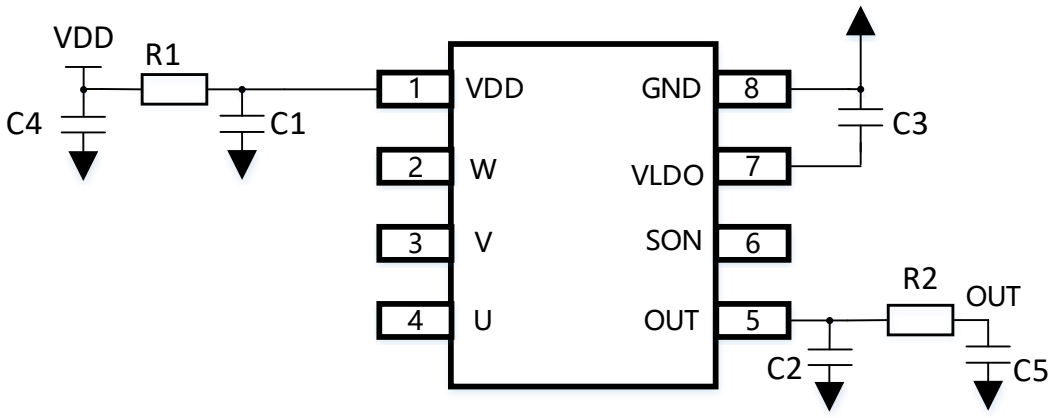


Figure 6.3 NSM3013 Application Circuit

Output	*Compact PCB routing*			*EMC robust PCB routing*			
Analog output	*Min*	*Type.*	*Max*	*Min*	*Type.*	*Max*	*备注*
C_1	100nF	100nF	1uF	47nF	100nF	1uF	
C_2	47nF	100nF	330nF	47nF	100nF	330nF	
C_3	47nF	100nF	220nF	47nF	100nF	220nF	
C_4	-	-	-	500pF	1nF	10nF	
C_5	-	-	-	500pF	1nF	10nF	
R_1	-	-	-	0Ω	10Ω	33Ω	
R_2	-	-	-	10Ω	50Ω	100Ω	

6.2. Default Angle Output

The Sensitive spot position of NSM301X is the center of chip. The magnet needs to be aligned with the center of the chip. The relationship between the angle of the chip output and the placement of the magnet is shown in the following figure:

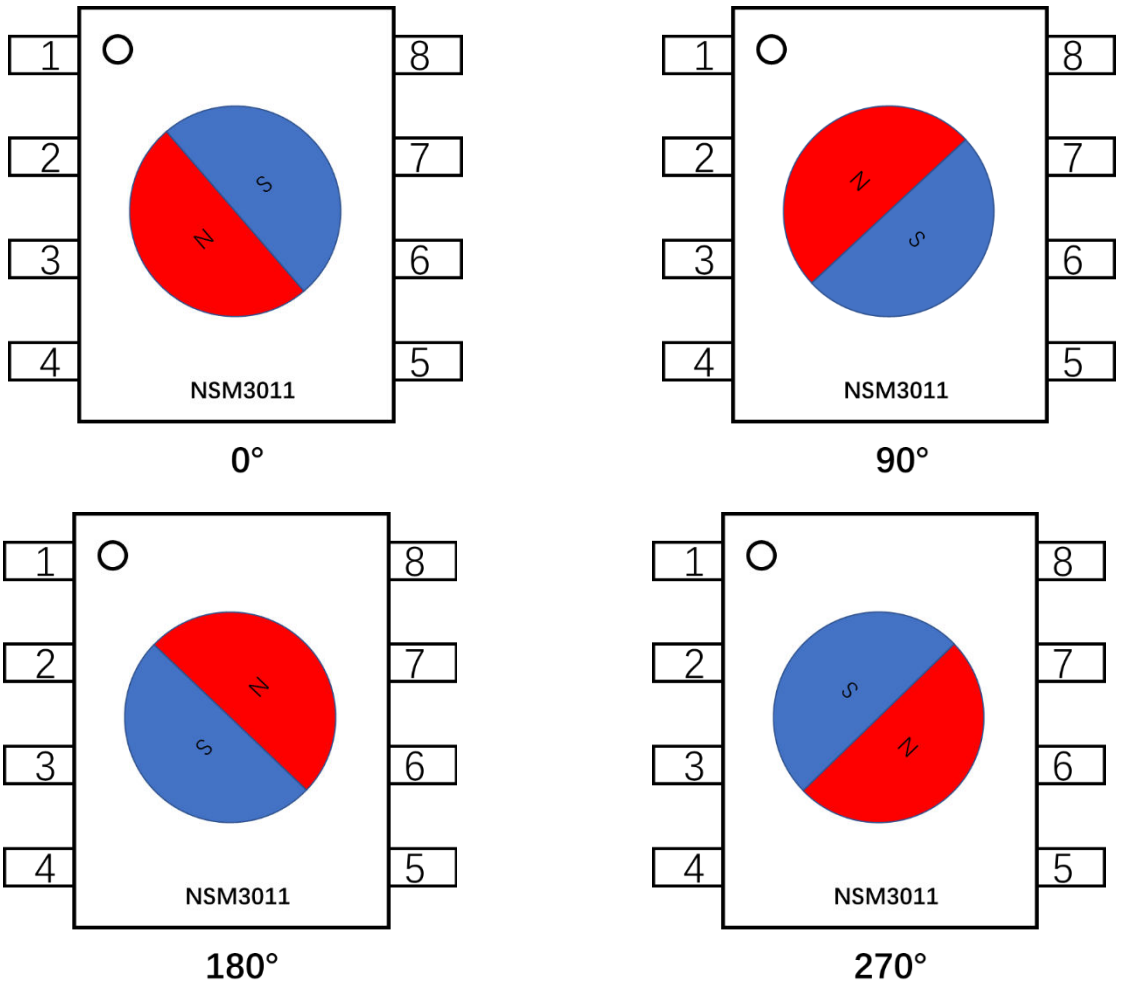
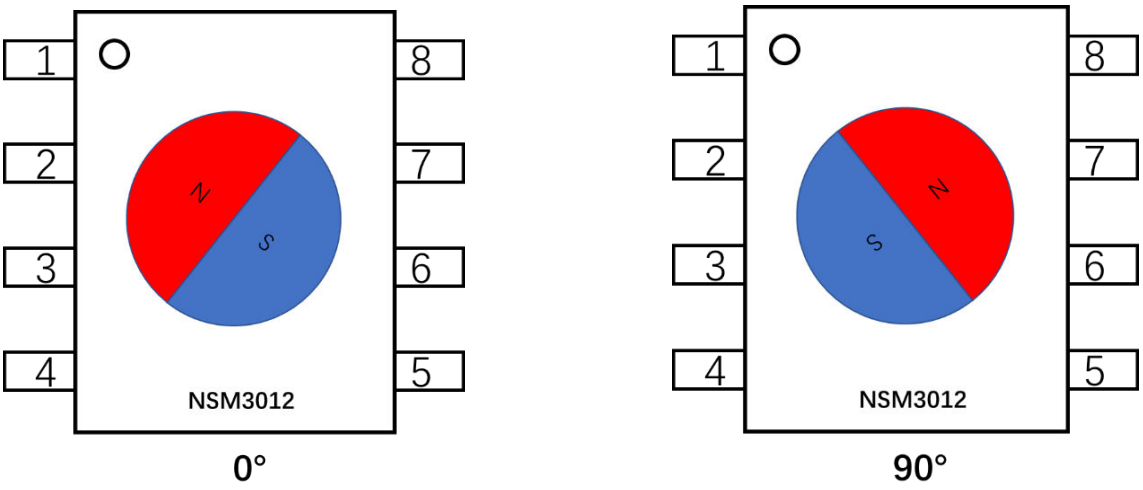


Figure 6.4 NSM3011 angle output in different placement



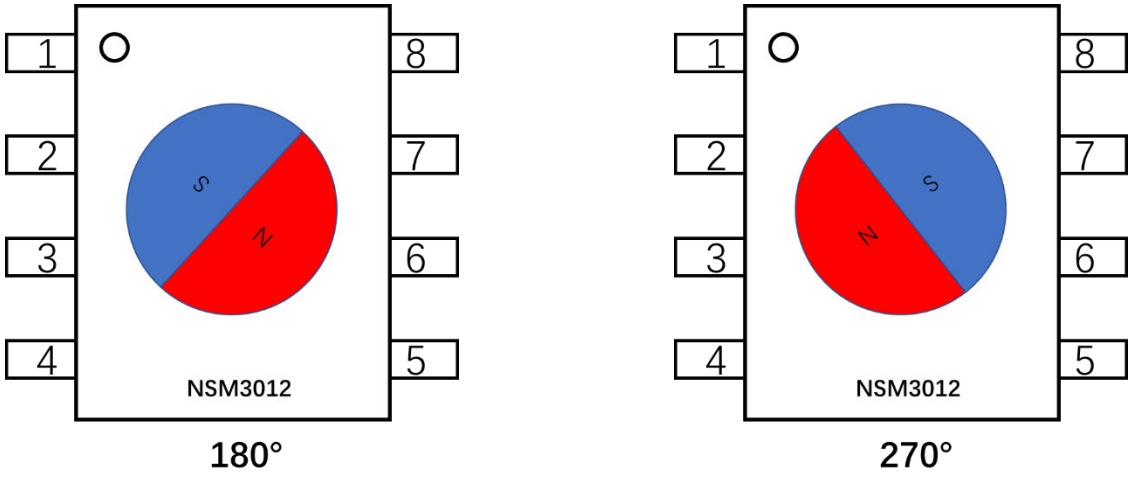
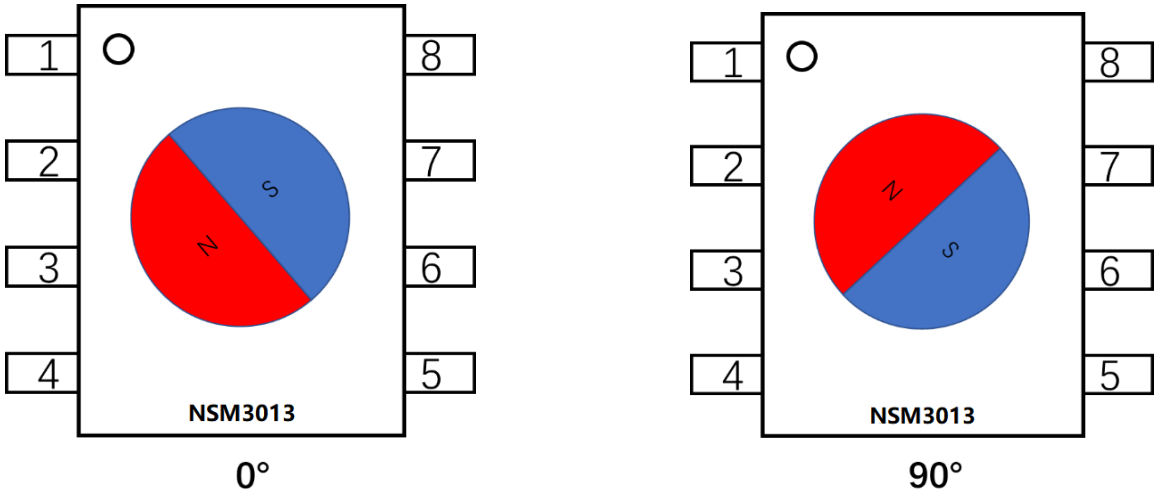


Figure 6.5 NSM3012 angle output in different placement



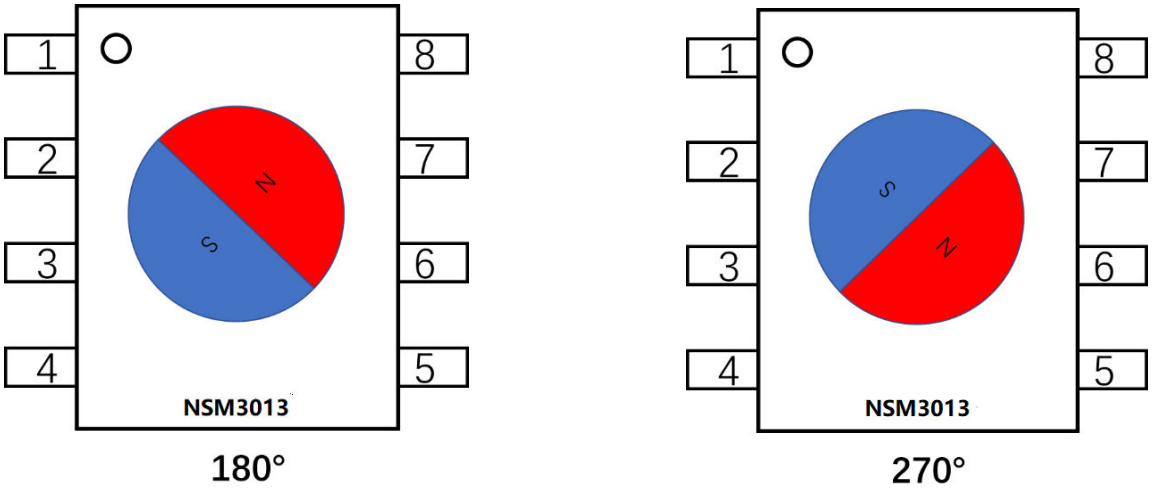
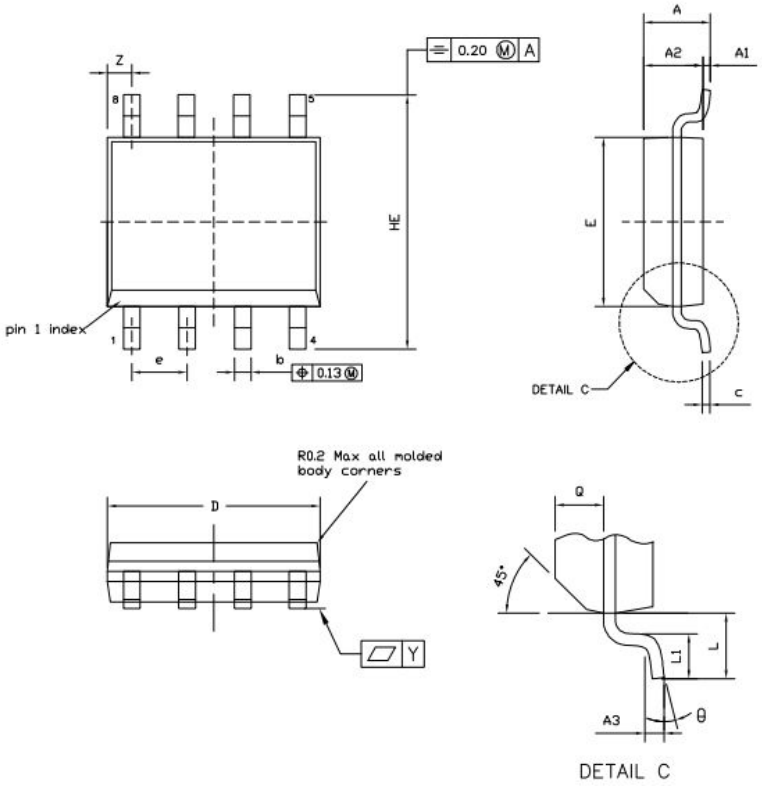


Figure 6.6 NSM3013 angle output in different placement

7. Package Information



✱ CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

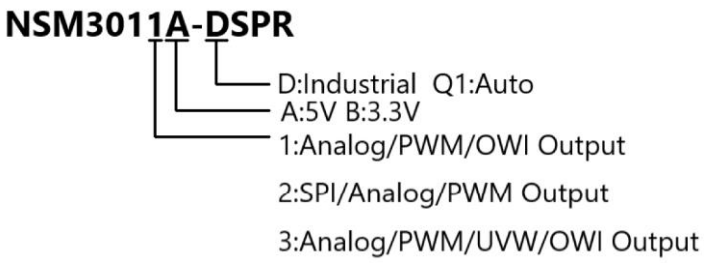
Figure 7.1 SOP8 Package Shape and Dimension in millimeters

8. Ordering Information

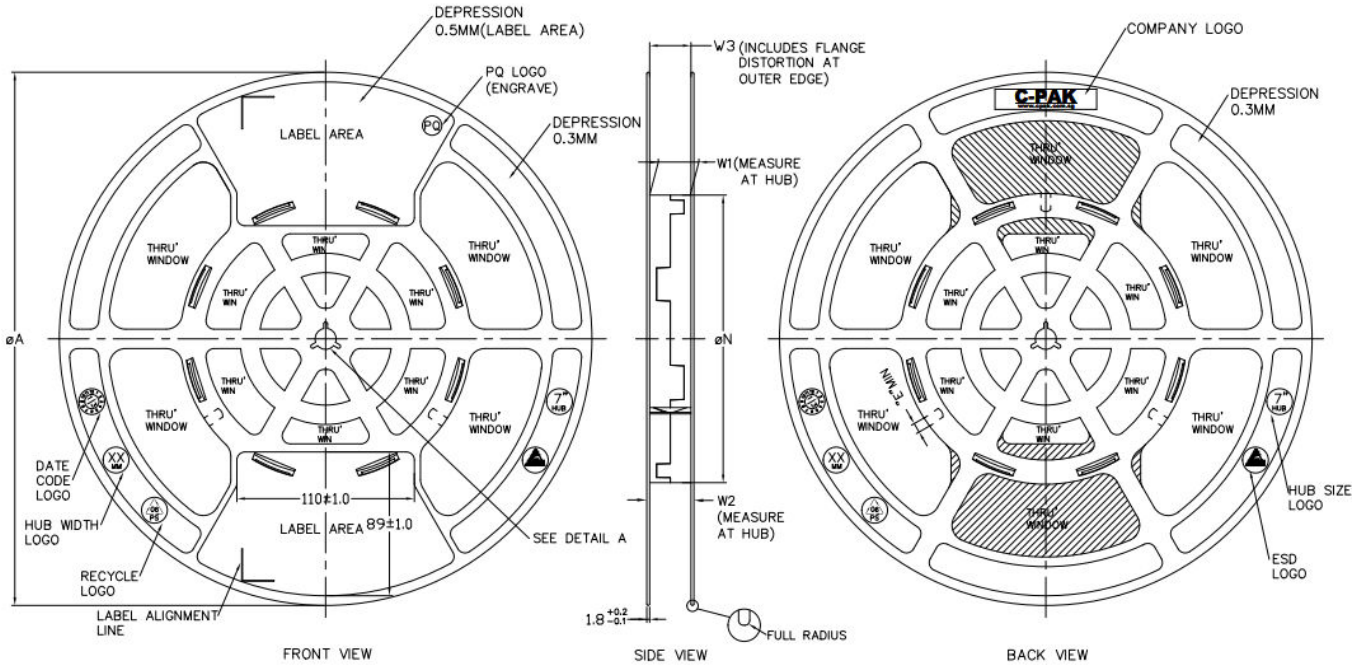
Order part number：

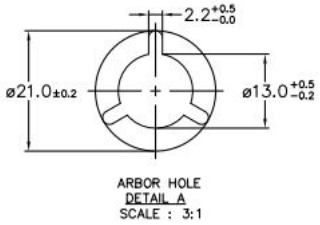
Part Number	*Power Supply*	*SPQ*	*MOQ*	*Package*
NSM3011A-DSPR	5V	2500	2500	SOP8
NSM3011A-Q1SPR	5V	2500	2500	SOP8
NSM3011B-DSPR	3.3V	2500	2500	SOP8
NSM3011B-Q1SPR	3.3V	2500	2500	SOP8
NSM3012A-DSPR	5V	2500	2500	SOP8
NSM3012A-Q1SPR	5V	2500	2500	SOP8
NSM3012B-DSPR	3.3V	2500	2500	SOP8
NSM3012B-Q1SPR	3.3V	2500	2500	SOP8
NSM3013A-DSPR	5V	2500	2500	SOP8
NSM3013A-Q1SPR	5V	2500	2500	SOP8
NSM3013B-DSPR	3.3V	2500	2500	SOP8
NSM3013B-Q1SPR	3.3V	2500	2500	SOP8

Part Number Rule:



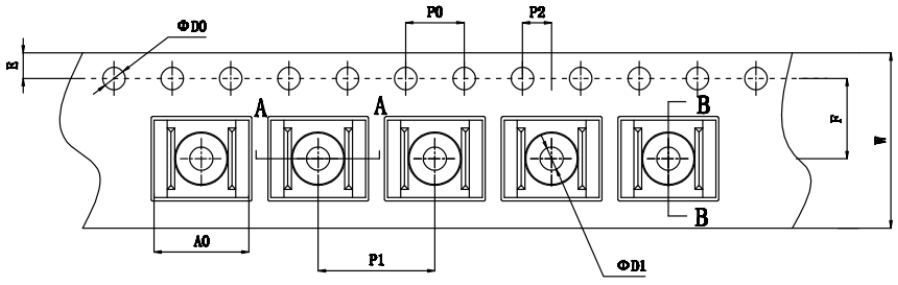
9. Tape and Reel Information

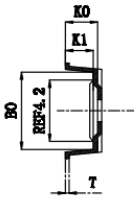


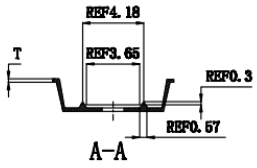


PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{9} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{6} & BELOW 10^{9}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES







Symbol	Spec (mm)
E	1.75±0.10
F	5.5±0.10
P2	2.00±0.10
D0	1.55±0.05
D1	1.6±0.10
P0	4.00±0.10
10P0	40.00±0.20

Symbol	Spec (mm)
W	12.00±0.30
P1	8.00±0.10
A0	6.50±0.10
B0	5.30±0.10
K0	2.20±0.10
K1	1.90±0.10
T	0.30±0.05

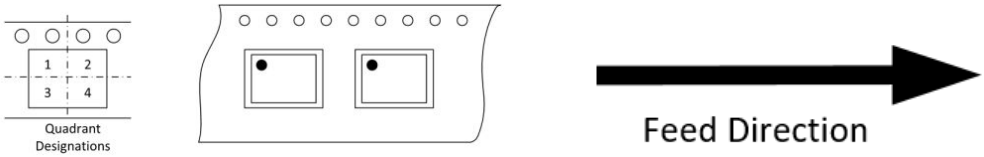


Figure 9.1 Tape and Reel Information of SOP8

10. Revision History

Revision	Description	Date
1.0	Initial Version	2022/5/7

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