NSC9262: Automotive Capacitive Sensor Conditioner with LIN Interface

Datasheet 1.2

Product Overview

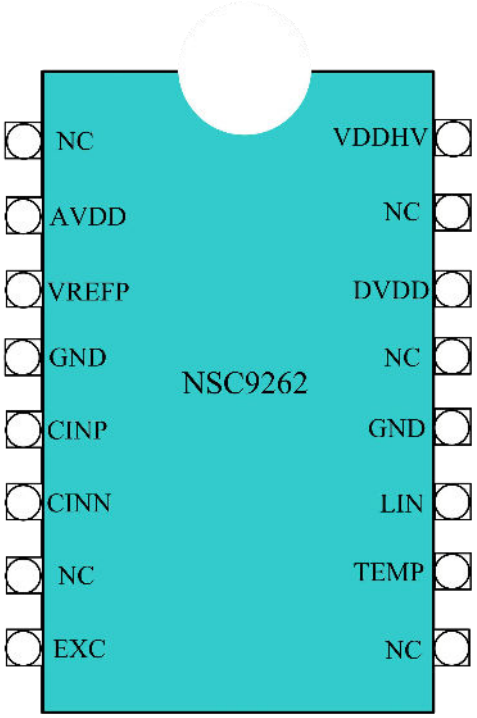
The NSC9262 is a highly integrated and AEC-Q100 qualified IC for capacitive sensor conditioning. The NSC9262 integrates a C/V converter, a 24-bit capacitance measurement channel, a 24-bit temperature measurement channel and sensor calibration logic. With the internal calibration algorithm built in the MCU, the NSC9262 supports to compensate the temperature drift of zero and span up to the 2nd order and also the linearity up to the 3rd order with calibration error less than 0.1%. The calibration coefficients are stored in a 57-byte EEPROM. The NSC9262 also supports Over-voltage and Reverse voltage protection. It can provide LIN output with sensor diagnostic function.

Key Features

- Over-voltage and Reverse voltage protection between -40V ~ 40V
- Power supply as high as 18V through VDDHV pin
- C/V converter with at most ± 16pF differential capacitor input
- 24-bit ADC for capacitance measurement
- 24-bit ADC for temperature measurement
- Internal and external temperature sensor supported
- Low drift voltage reference
- 1X~8X ADC digital gain
- Sensor calibration logic with built-in MCU
- 57-byte EEPROM
- Dedicated OWI communication
- LIN interface communication up to 20kbit/s
- Compliant with LIN Specifications 1.3, 2.0, 2.1 and 2.2
- Bare die or RoHS-compliant package:
  SSOP16 (30mm^2)
- AEC-Q100 qualified
- Operation temperature: -40°C~150°C

Applications

- Capacitive sensors
- Automotive braking system
- Automotive air-conditioner



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1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply voltage	VDDHV	-0.5		40	V	
Withstand voltage to ground (LIN)	V_{LIN}	-40		40	V	
AVDD output	AVDD	-0.3		6.5	V	
Analog pins voltage		-0.3		AVDD+0.3	V	
Analog output current limit				25	mA	
Digital pins voltage		-0.3		AVDD+0.3	V	25℃
ESD susceptibility	HBM	±1.5			kV	According to AEC-Q100-002 RevE
	CDM	±500			V	
Maximum junction temperature	Tjmax			155	℃	
Storage temperature		-60		150	℃	
Operation temperature	T_{A_EXT}	-40		150	℃	Normal temperature range

2.0 ELECTRICAL CHARACTERISTICS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply and Regulation						
Supply voltage Range	VDDHV	7	12	18	V	
AVDD Output	AVDD		5		V	
DVDD LDO Output	DVDD	1.75	1.8	1.85	V	
Power On Reset	V_{POR_AVDD}		2.5		V	POR threshold as power up
	V_{POR_HYS}		0.1		V	POR Hysteresis
Operation Current	I_{avdd}		1.9		mA	
Standby Current	I_{sleep}		95		μA	25℃
Reference Voltage and Current Source						
VREF Output	VREF		2		V	
VREF Current Limit	I_{VREF_limit}		20		mA	Short to Ground
Capacitance Measurement Channel						
Differential Input	C_{RANGE}		±16		pF	CV_RANGE<1:0>=2'b00

Capacitance Range			±12		pF	CV_RANGE<1:0>=2'b01
			±8		pF	CV_RANGE<1:0>=2'b10
			±4		pF	CV_RANGE<1:0>=2'b11
Common Mode Capacitance Range	C_{CM_RANGE}		48		pF	CV_RANGE<1:0>=2'b00
			36		pF	CV_RANGE<1:0>=2'b01
			24		pF	CV_RANGE<1:0>=2'b10
			24		pF	CV_RANGE<1:0>=2'b11
CAPDAC Range		0		63.5	pF	0.5pF/LSB
PADC Resolution	RESRAW		24		Bits	
PADC Output Data Rate	ODR_P	5		4800	Hz	
PADC ENOB	ENOB_P	Refer to Table 4.1			Bits	Depends on ODR_P
Excitation Source (EXC)						
Excitation Frequency	CV_FREQ		76.8		kHz	
Excitation Voltage Amplitude	VAC		2	2.2	V	
Drivability	DRV		50		pF	Allow ground capacitance
Temperature Measurement Channel (Internal and External Temperature Sensor)						
TADC Resolution	RES_T	24			Bit	
TADC GAIN	GAIN_T	1		4		1,2,4
TADC Output Data Rate	ODR_T	5		4800	Hz	
TADC ENOB	ENOB_P	Refer to Table 4.3				
Error of Internal Temperature Sensor			±1	±2	℃	-40 to 125 ℃
TEMP Input Impedance			1		Gohm	
LIN Interface						
Input Low Level Voltage Receiver	V_{RECL}			0.4	VDDHV	
Input High Level Voltage Receiver	V_{RECH}	0.6			VDDHV	
Input Hysteresis Receiver	V_{RECHYS}	0.08		0.12	VDDHV	$V_{RECHYS} = V_{RECH} - V_{RECL}$
Input Center Point Receiver	V_{BUS_CNT}	0.475	0.5	0.525	VDDHV	$V_{BUS\_CNT} = (V_{RECH} + V_{RECL})/2$
Output Low Level Voltage Transmitter	V_{LINL}	0.6	1.2	2.0	V	
Output High Level Voltage Transmitter	V_{LINH}	0.9		1	VDDHV	

Pull Up resistance VDDHV to LIN	R_{LINPU}	20	30	47	kOhm	in series with diode to VDDHV
Output Capacitance LIN	C_{LIN_OUT}			250	pF	
Output Current Limitation LIN Output Driver	I_{LIM}	40	90	200	mA	Sink, driver on, V_{LIN} = VDDHV
Input Current LIN Dominant	$I_{LINPASdom}$	-1			mA	V_{LIN} = 0V, VDDHV = 12V Driver off
Input Current LIN Recessive	$I_{LINPASrec}$		3	20	µA	V_{LIN} ≥ VDDHV 7V ≤ V_{LIN} ≤18V 7V ≤ VDDHV ≤18V Driver off
Input Current LIN Lost GND	I_{LIN_NOGND}	-1		1	mA	0V ≤V_{LIN}≤18V VDDHV = 12V Lost GND
Input Current LIN Lost Supply				20	µA	0V ≤V_{LIN}≤18V VDDHV = 0V
Voltage Drop over Pull Up Diode	$V_{SerDiode}$	0.4	0.7	1	V	
TXD Timeout	$t_{TXDTIMEOUT}$	10	19	30	ms	
Slew Rate (Rising and Falling Edges)	SR_{LIN}	0.5	1.3	3	V/us	Refer to Figure 2.1
Propagation Delay Receiver:LIN low -> RXD low	$t_{RXDLINL}$	2	4	6	us	Refer to Figure 2.2
Propagation Delay Receiver:LIN high-> RXD high	$t_{RXDLINH}$	2	4	6	us	Refer to Figure 2.2
Symmetry of Receiver Propagation Delay	$t_{RXDLINSYM}$	-2		2	us	$t_{RXDLINH}$ - $t_{RXDLINL}$
Symmetry of Transmitter Propagation Delay	$t_{TXDLINSYM}$	-2		2	us	$t_{TXDLINL}$ - $t_{TXDLINH}$
Diagnostic and Alarm						
Over Temperature Protection	T_{OT}	170	180		℃	
VDDHV Over Voltage	$V_{OVDetThres}$		35		V	
VDDHV Under Voltage	$V_{UVDetThres}$		6		V	
OSC						
ADC Clock	FOSC_MOD		1.2		MHz	

Clock Rate Error	FOSC_ERR	-1%		1%		-40~125℃
EEPROM						
Programming Temperature	T_{EEP}	-25		105	℃	
Endurance	N_{EEP}	500				
Programming Time	t_{EEP}		800		ms	
Date Retention	t_{DR}	10			year	150℃
Serial Interface						
OWI Bit Period	Towi	0.02		4	ms	
OWI Pull-up Resistance	Rowi_pu	300			Ohm	

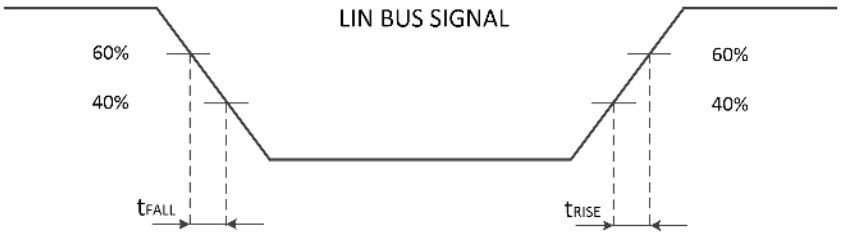


Figure 2.1 t_{FALL} and t_{RISE}

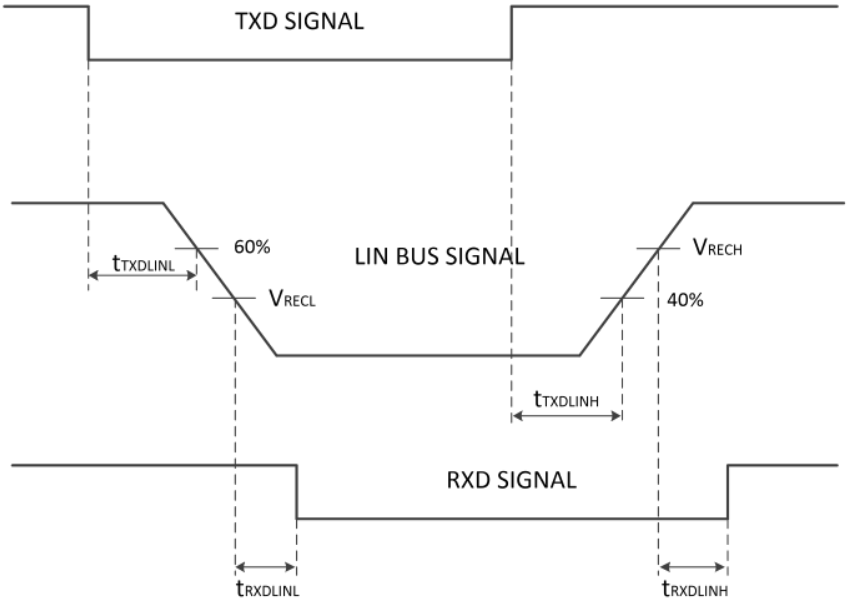


Figure 2.2 $t_{TXDLINSYM}$ and $t_{RXDLINSYM}$

3.0 REGISTER DESCRIPTION

The register map of the NSC9262 includes two parts, normal registers and EEPROM registers. The normal registers include data registers and some control registers, while the EEPROM registers are mainly configuration registers and calibration coefficients. All EEPROM registers should be written through external interface in command mode (register 'CMD' = '0x00').

3.1. NORMAL REGISTERS

SOFT_RESET (R/W)

Addr	Bit	Register name	Default	Description
0x00	5，2	SOFTRESET	0x00	Set either of these two bits to 1 to reset the chip. Return to 0 after reset.

ERROR_STATUS (Read only)

Addr	Bit	Register name	Default	Description
0x02	7 – 3	Reserved	5'b00000	Reserved
	2	CRC_ERR	1'b0	1: CRC error detected during EEPROM loading; When CRC error is asserted, EEPROM register bits 'OWI_DIS', 'EEPROM_LOCK' are forced to 0.
	1	LOADING_END	1'b0	1: EEPROM loading end flag
	0	ROM_CHECK_ERR	1'b0	1: ROM check error flag

PDATA (Read only, Primary channel data register)

Addr	Bit	Register name	Default	Description
0x06	7 – 0	PDATA<23:16>	0x00	Signed，2's complement: When 'RAW_P'= 1, stores the ADC output of primary channel, When 'RAW_P'= 0, stores the calibrated primary channel data.
0x07	7 – 0	PDATA<15:8>	0x00	
0x08	7 – 0	PDATA<7:0>	0x00	

TDATA (Read only, temperature channel data register)

Addr	Bit	Register name	Default	Description
0x09	7 – 0	TDATA<23:16>	0x00	Signed，2's complement: When 'RAW_T' = 1, stores the ADC output of temperature channel, When 'RAW_T'= 0, stores the calibrated temperature data, LSB = 1/2^16℃. Real Temperature =TDATA/2^16+25℃
0x0a	7 – 0	TDATA<15:8>	0x00	
0x0b	7 – 0	TDATA<7:0>	0x00	

COMMAND (R/W, command register)

Addr	Bit	Register name	Default	Description
0x30	7 – 0	CMD<7:0>	0x03	0x00: command mode, all EEPROM can be written only in command mode. 0x03: Active mode 0x23: Enter EEPROM program mode

QUIT_OWI (Write only)

Addr	Bit	Register name	Default	Description
0x61	7 – 0	QUIT_OWI<7:0>	0x00	Write'0x5D' to this register to quit OWI communication

EE_PROG (R/W)

Addr	Bit	Register name	Default	Description
0x6a	7 – 0	EE_PROG<7:0>	0x00	Write '0x3E / 0xBE' to this register to start EEPROM Programming. Automatically cleared to '0x00' after programming finished. 0x3E: EEPROM erased by byte 0xBE: EEPROM erased by bank

3.2. EEPROM REGISTERS

SYS_CONFIG (R/W)

Addr	Bit	Register name	Default	Description
0xa1	7	CAL_MODE	1'b0	0: one segment calibration with the 2nd order temperature coefficients 1: two segment calibration with the 1st order temperature coefficients.
	6 - 3	Reserved	4'b0000	Reserved
	2	LIN_PID2_en	1'b0	0: disable LIN Product Identification – PID2 (internal use); 1: enable LIN Product Identification – PID2 (internal use)
	1	OWI_DIS	1'b0	1: OWI disabled (Won't be effective until next power on reset or soft reset after EEPROM is programmed)
	0	Reserved	1'b0	Reserved

OUTPUT_CONFIG (R/W)

Addr	Bit	Register name	Default	Description
0xa2	7 - 6	LIN_version	2'b00	00: LIN version1.3; 01: LIN version1.3; 10: LIN version2.0; 11: LIN version2.1(2.2)
	5	LIN_save_config_dis	1'b0	0: enable saving configuration to EEPROM through LIN; 1: disable saving configuration to EEPROM through LIN
	4	LIN_sleep_mode_dis	1'b0	0: enable sleep mode; 1: disable sleep mode
	3	LIN_sample_point	1'b0	0: 3 samples/bit 1: 5 samples/bit
	2 - 0	Reserved	3'b000	Reserved

CV_CONFIG (R/W)

Addr	Bit	Register name	Default	Description
0xa3	7	Reserved	1'b0	Reserved. Should be 0
	6 – 0	CAPOFF<6:0>	7'b0000000	Set internal CAPDAC offset for input CAPOFF = CAPOFF<6:0>*0.5pF

PCH_Config1 (R/W)

Addr	Bit	Register name	Default	Description

0xa4	7 – 6	Reserved	2’b00	Reserved. Should be 2’b00
	5 – 4	CV_RANGE<1:0>	2’b00	00: C_{RANGE} = ±16pF, C_{CM_RANGE} = 48pF； 01: C_{RANGE} = ±12pF, C_{CM_RANGE} = 36pF； 10: C_{RANGE} = ±8pF, C_{CM_RANGE} = 24pF； 11: C_{RANGE} = ±4pF, C_{CM_RANGE} = 24pF；
	3 – 0	ODR_P<3:0>	4’b0000	PADC Output Data Rate Setting 0000: 4.8KHz, 0001: 2.4KHz, 0010: 1.2KHz, 0011: 600Hz, 0100: 300Hz, 0101: 150Hz, 0110: 75Hz, 0111: 37.5Hz, 1000: 20Hz(with 60Hz notch), 1001: 20Hz（with 50Hz notch）, 1010: 10Hz（with 60Hz notch）, 1011: 10Hz（with 50Hz notch）, 1100: 5Hz（with 60Hz notch）, 1101: 5Hz (with 50Hz notch), 1110,1111: PADC disabled

PCH_Config2 (R/W)

Addr	Bit	Register name	Default	Description
0xa5	7 – 6	DIG_GAIN<1:0>	2’b00	Digital gain configuration 00: 1X, 01:2X, 10: 4X, 11: 8X
	5 – 1	Reserved	5’b00000	Reserved. Should be 0
	0	RAW_P	1’b0	0: update calibrated sensor data into ‘PDATA’ register. 1: update raw primary ADC data into 'PDATA' register after conversion.

TCH_Config (R/W)

Addr	Bit	Register name	Default	Description
0xa6	7	EXT_TEMP	1’b0	0: internal temperature sensor selected 1: external temperature sensor selected (TEMP pin as external temperature sensor input)
	6 – 5	GAIN_T<1:0>	2’b00	Gain for external temperature channel 00:1X, 01:2X, 10/11:4X
	4 – 1	ODR_T	4’b0000	TADC output data rate，similar as ODR_P 0000:4.8KHz, 0001: 2.4KHz, 0010: 1.2KHz, 0011: 600Hz, 0100: 300Hz, 0101: 150Hz, 0110: 75Hz, 0111: 37.5Hz, 1000: 20Hz(with 60Hz notch), 1001: 20Hz（with 50Hz notch）, 1010: 10Hz（with 60Hz notch）, 1011: 10Hz（with 50Hz notch）, 1100: 5Hz（with 60Hz notch）, 1101: 5Hz (with 50Hz notch) , 1110,1111: TADC disabled
	0	RAW_T	1’b0	1: store the direct TADC output into ‘TDATA’ register 0: store the calibrated TADC data into ‘TDATA’ register.

CLAMPH (R/W)

Addr	Bit	Register name	Default	Description
0xa7	7 – 0	CLAMPH<7:0>	0x00	Set clamping high level.

CLAMPL (R/W)

Addr	Bit	Register name	Default	Description
0xa8	7 – 0	CLAMPL<7:0>	0x00	Set clamping low level.

OFFSET0 (R/W)

Addr	Bit	Register name	Default	Description
0xa9	7 – 0	OFF0<15:8>	0x00	Sensor Calibration coefficient, offset at T0. LSB=1/2^15. RANGE (-1, +1)
0xaa	7 – 0	OFF0<7:0>	0x00	

CTC1 (R/W)

Addr	Bit	Register name	Default	Description
0xab	7 – 0	CTC1<15:8>	0x00	Sensor Calibration coefficient, CAL_MODE=0: the 1st order temperature coefficient of offset. LSB=1/2^22. RANGE (-0.00781, +0.00781) CAL_MODE=1: the 1st order temperature coefficient of offset for segment 0.LSB=1/2^22. RANGE (-0.00781, +0.00781)
0xac	7 – 0	CTC1<7:0>	0x00	

CTC2 (R/W)

Addr	Bit	Register name	Default	Description
0xad	7 – 0	CTC2<15:8>	0x00	Sensor Calibration coefficient, CAL_MODE=0: the 2nd order temperature coefficient of offset. LSB=1/2^29, RANGE (-6.1e-5, +6.1e-5) CAL_MODE=1: the 1st order temperature coefficient of offset for segment 1, LSB=1/2^22. RANGE (-0.00781, +0.00781)
0xae	7 – 0	CTC2<7:0>	0x00	

S0 (R/W)

Addr	Bit	Register name	Default	Description
0xaf	7 – 0	S0<15:8>	0x00	Sensor calibration coefficient, sensitivity at T0. LSB=1/2^15 (unsigned), RANGE (0, 2)
0xb0	7 – 0	S0<7:0>	0x00	

STC1 (R/W)

Addr	Bit	Register name	Default	Description
0xb1	7 – 0	STC1<15:8>	0x00	Sensor Calibration coefficient, CAL_MODE=0: the 1st order temperature coefficient of sensitivity. LSB=1/2^22. RANGE (-0.00781, +0.00781) CAL_MODE=1: the 1st order temperature coefficient of sensitivity for segment 0. LSB=1/2^22. RANGE (-0.00781, +0.00781)
0xb2	7 – 0	STC1<7:0>	0x00	

STC2 (R/W)

Addr	Bit	Register name	Default	Description
0xb3	7 – 0	STC2<15:8>	0x00	Sensor Calibration coefficient. CAL_MODE=0: the 2nd order temperature coefficient of sensitivity. LSB=1/2^29, RANGE (-6.1e-5, +6.1e-5) CAL_MODE=1: the 2nd order temperature coefficient of sensitivity for segment 1, LSB=1/2^22. RANGE (-0.00781, +0.00781)
0xb4	7 – 0	STC2<7:0>	0x00	

KS (R/W)

Addr	Bit	Register name	Default	Description

0xb5	7 – 0	KS<15:8>	0x00	Sensor calibration coefficient, the 2nd order nonlinearity coefficient, LSB=1/2^15, RANGE (-1, +1)
0xb6	7 – 0	KS<7:0>	0x00	

KSS (R/W)

Addr	Bit	Register name	Default	Description
0xb7	7 – 0	KSS<15:8>	0x00	Sensor calibration coefficient, the 3rd order nonlinearity coefficient, LSB=1/2^16, RANGE (-0.5, +0.5)
0xb8	7 – 0	KSS<7:0>	0x00	

SUPPLIER_ID (R/W)

Addr	Bit	Register name	Default	Description
0xb9	7 – 0	SUPPLIER_ID<15:8>	0x00	LIN Product Identification – Supplier ID
0xba	7 – 0	SUPPLIER_ID<7:0>	0x00	

FUNCTION_ID (R/W)

Addr	Bit	Register name	Default	Description
0xbb	7 – 0	FUNCTION_ID<15:8>	0x00	LIN Product Identification – Function ID
0xbc	7 – 0	FUNCTION_ID<7:0>	0x00	

VARIANT_ID (R/W)

Addr	Bit	Register name	Default	Description
0xbd	7 – 0	VARIANT_ID<7:0>	0x00	LIN Product Identification – Variant ID

LIN_NAD (R/W)

Addr	Bit	Register name	Default	Description
0xbe	7 – 0	LIN_NAD<7:0>	0x00	LIN node address – LIN NAD

T0 (R/W)

Addr	Bit	Register name	Default	Description
0xbf	7 – 0	T0<7:0>	0x00	Sensor calibration coefficient, reference temperature point, Real reference temperature, REAL_T0 = T0 + 25, LSB=1. RANGE (-128, +127)

KTS (R/W)

Addr	Bit	Register name	Default	Description
0xc0	7 – 0	KTS<7:0>	0x00	Sensor calibration coefficient, the 2nd order nonlinearity coefficient for external temperature sensor, LSB=1/2^7, RANGE (-1, +1)

MTO (R/W)

Addr	Bit	Register name	Default	Description
0xc1	7 – 0	MTO<15:8>	0x00	Sensor calibration coefficient, offset coefficient of external temperature sensor , MTO: LSB=1/2^15, RANGE (-1, +1)
0xc2	7 – 0	MTO<7:0>	0x00	

KT (R/W)

Addr	Bit	Register name	Default	Description
0xc3	7 – 0	KT<15:8>	0x00	Sensor calibration coefficient: sensitivity coefficient of external temperature sensor, KT: LSB=1/2^12, RANGE (-8, +8)
0xc4	7 – 0	KT<7:0>	0x00	

TEMP_THRES (R/W)

Addr	Bit	Register name	Default	Description
0xc5	7 – 0	TEMP_THRES_H<7:0>	0x00	Upper limit of temperature data
0xc6	7 – 0	TEMP_THRES_L<7:0>	0x00	Lower limit of temperature data

SPARE (R/W)

Addr	Bit	Register name	Default	Description
0xc7	7 – 0	SPARE1<7:0>	0x00	Spare register 1
0xc8	7 – 0	SPARE2<7:0>	0x00	Spare register 2
0xd5	7 – 0	SPARE3<7:0>	0x00	Spare register 3
0xd6	7 – 0	SPARE4<7:0>	0x00	Spare register 4

PADC_OFF (R/W)

Addr	Bit	Register name	Default	Description
0xc9	7 – 0	PADC_OFF<23:16>	0x00	PADC calibration coefficient: PADC offset, LSB=1/2^23，RANGE (-1, +1)
0xca	7 – 0	PADC_OFF<15:8>	0x00	
0xcb	7 – 0	PADC_OFF<7:0>	0x00	

PADC_GAIN (R/W)

Addr	Bit	Register name	Default	Description
0xcc	7 – 0	PADC_GAIN<15:8>	0x00	PADC calibration coefficient: PADC gain, LSB=1/2^16，RANGE (-0.5, +0.5)
0xcd	7 – 0	PADC_GAIN<7:0>	0x00	

P0 (R/W)

Addr	Bit	Register name	Default	Description
0xce	7 – 0	P0 <7:0>	0x00	Sensor calibration coefficient: reference pressure point for nonlinearity calibration, LSB=1/2^7, RANGE (-1, +1)

SERIAL_NUMBER (R/W)

Addr	Bit	Register name	Default	Description
0xcf	7 – 0	SERIAL_NUMBER<31:24>	0x00	LIN Product Identification – Serial Number
0xd0	7 – 0	SERIAL_NUMBER <23:16>	0x00	
0xd1	7 – 0	SERIAL_NUMBER <15:8>	0x00	
0xd2	7 – 0	SERIAL_NUMBER <7:0>	0x00	

MESSAGE_ID1 (R/W)

Addr	Bit	Register name	Default	Description
0xd3	7 – 0	MESSAGE_ID1<15:8>	0x00	LIN Product Identification – Message ID1

0xd4	7 – 0	MESSAGE_ID1<7:0>	0x00	Only for PID1

PID1 (R/W)

字节地址	位地址	寄存器名称	默认值	描述
0xd7	7 – 0	PID1<7:0>	0x00	LIN Product Identification – PID1

PID2 (R/W)

Addr	Bit	Register name	Default	Description
0xd8	7 - 0	PID2<7:0>	0x00	LIN Product Identification – PID2 (internal use)

EEPROM_LOCK (R/W)

Addr	Bit	Register name	Default	Description
0xd9	7	EEPROM_LOCK	1'b0	1: EEPROM lock，set 1 and then EEPROM can't be programmed. (Won't be effective until next power on reset or soft reset after EEPROM is programmed)
	6 – 0	PartID (read only)	7'b0001001	NOVOSENSE chip ID

4.0 FUNCTION DESCRIPTION

The NSC9262 is a highly integrated and AEC-Q100 qualified sensor conditioner for capacitive sensors. The chip supports Over-voltage and Reverse voltage protection. LIN output compliant with Specification 1.3/2.0/2.1/2.2 is available, high voltage power supplied directly through VDDHV. The NSC9262 uses differential inputs with at most ±16pF differential input capacitance range and 76.8pF common mode capacitance range. The chip incorporates five parts: analog front-end module, digital module, LIN interface module, power supply module and serial interfaces. The block diagram of the NSC9262 is shown in Figure 4.1.

Analog front-end module includes a primary signal measurement channel with a C/V converter followed by a 24-bit ∑Δ ADC, a temperature measurement channel with also a 24-bit ∑Δ ADC, for precision sensor signal and temperature measurement.

The digital module is composed of registers, EEPROM, control logic, and a built-in MCU. The sensor calibration algorithm is implemented with the built-in MCU and can supports up to 2nd order temperature drift compensation of offset and sensitivity for the sensor. It can also compensate the nonlinearity of sensor output up to 3rd order. The configuration parameters and coefficients for calibration are stored in the EERPOM of 57 bytes.

The LIN interface module includes LIN protocol control part and LIN physical transceiver part, compatible with LIN Specification 1.3//2.0/2.1/2.2. Meanwhile it supports diagnostic function of Class I.

The power supply module includes a high precision voltage reference, a sensor voltage driver, over-voltage and reverse voltage protection block.

The NSC9262 supports OWI serial interface, writing and reading registers of configuration, calibration coefficients and data. Through the highly integrated and flexible interface, the NSC9262 only needs one wire to realize sensor calibration, field verification and full scale range modification.

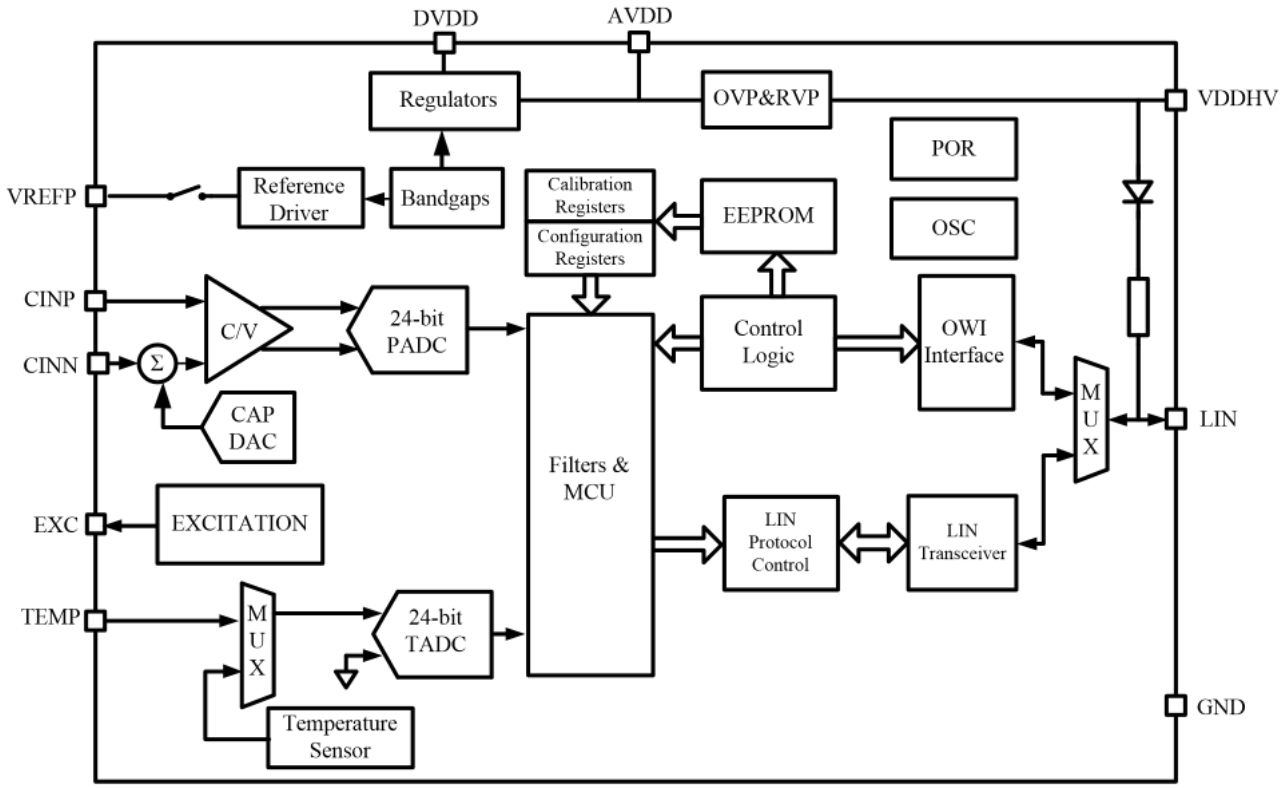


Figure 4.1 Block diagram of the NSC9262

4.1. ANALOG FRONT-END MODULE 1： PRIMARY SIGNAL CHANNEL

4.1.1. Capacitance measurement mode

The NSC9262 generates a square wave at EXC pin with 76.8KHz frequency and 2V amplitude, which is used to drive input capacitor.

As shown in Figure 4.2, where the external input capacitors are connected. The differential input capacitors' common plate is driven by the square wave at EXC pin. Since the voltage at CINP and CINN keeps constant, the input parasitic capacitance would not affect the output.

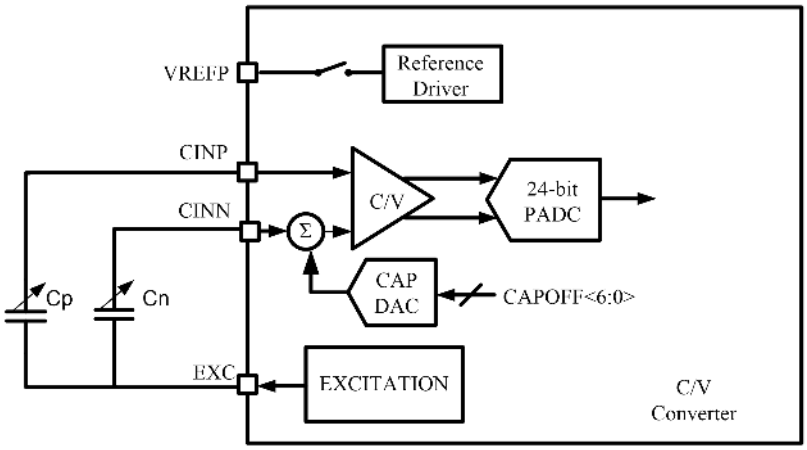


Figure4.2 C/V converter

4.1.2. The measurement range of C/V converter

4.1.2.1. The differential input capacitance range

The PADC converts the analog output of C/V converter to digital output, which is filtered by digital filter with 24-bit digital output $PDATA_{RAW}$. $PDATA_{RAW}$ is expressed by,

$$PDATA_{RAW} = \frac{Cp - Cn - CAPOFF}{|C_{RANGE}|} * 2^{23}$$

CAPOFF is an internal offset compensated capacitance configured by CAPOFF<6:0>. The unit capacitance of CAPDAC is 0.5pF, so it's as large as 127*0.5pF = 63.5pF. C_{RANGE} is the full scale range of C/V measurement configured by CV_RANGE<1:0> as referred to Section 3.2. $PDATA_{RAW}$ can be read from P channel data registers (Reg0x06，07，08) when RAW_P = 1. When RAW_P = 0, the built-in MCU will calibrate the sensor using sensor calibration coefficients and the data of temperature measurement. So the content of PDATA registers are the sensor output after temperature calibration.

4.1.2.2. The common mode capacitance range

When the differential input capacitance is not out of range (PDATAraw is in between ±1), the common mode capacitance range is related to VREF and CV_RANGE<1:0> as referred to Section 3.2.

4.1.3. Digital filter

The bandwidth and output data rate (ODR) of the digital filter can be set by 'ODR_P'. ODR can be set from 4.8 KHz to 5 Hz. The lower ODR, the lower noise the PADC output will have, in the cost of slower time response. Table 4.1 shows the effective number of bits (ENOB) of PADC output with different ODR_P settings. The relationship of ENOB with RMS noise is:

$$ENOB_{RMS} = 24 - \log_2(RMS_{ADC})$$

RMS_{ADC} is the RMS value of ADC output noise in LSB. The relationship between RMS ENOB ($ENOB_{RMS}$) and noise free ENOB ($ENOB_{NF}$) is shown as below:

$$ENOB_{NF} = ENOB_{rms} - 2.7$$

Table 4.1 $ENOB_{RMS}$ of PADC under different ODR settings

ODR_P(Hz)	C_{RANGE}=±16pF	C_{RANGE}=±12pF	C_{RANGE}=±8pF	C_{RANGE}=±4pF
4800	15.6	15.7	16.0	15.9
2400	15.9	15.9	16.2	16.0
1200	16.3	16.2	16.7	16.6
600	16.7	16.6	17.1	17.0
300	17.1	17.2	17.6	17.4
150	17.6	17.6	18.0	17.8
75	18.1	18.1	18.5	18.4
37.5	18.6	18.6	19.1	18.7
20	19.0	19.1	19.4	19.3
10	19.6	19.5	19.9	19.8
5	20.1	20.0	20.4	20.1

4.2. ANALOG MODULE 2: TEMPERATURE MEASUREMENT CHANNEL

The temperature measurement channel is to measure the working temperature of the sensor for the temperature compensation of the sensed signal. This channel works independently of the capacitance measurement channel. The NSC9262 supports both internal temperature sensor and external temperature sensor, selected by register bit 'EXT_TEMP' bit. The temperature sensor's output is digitized by a 24-bit ADC (TADC) and also digital filtered. The ODR setting of the temperature measurement channel is the same as the primary signal channel, set by 'ODR_T'. When the temperature difference between the sensor element and the NSC9262 chip is acceptable, internal temperature sensor can be used. Otherwise, a proper external temperature measurement scheme should be chosen, such as diode, RTD, NTC or the bridge resistor itself, etc. Through different 'RAW_T' setting, either the direct TADC data or the calibrated temperature data can be read from 'TDATA' registers.

4.2.1. Internal temperature sensor

The internal temperature sensor is factory calibrated, with its calibration coefficients stored at EEPROM registers reg0xC1, reg0xC2 and reg0xC3. When 'RAW_T' is set to 0 and 'GAIN_T' is set to 4X, the NSC9262 can provide a temperature reading in degree Celsius, in the format of

$$T = TDATA / 2\text{^}16 + 25\ ℃$$

For example, 'TDATA=0x1FF24B' corresponding to 56.95˚C. The relationship between the noise of the internal temperature sensor and 'ODR_T' setting is shown in Table 4.2.

Table 4.2 RMS Noise of Internal Temperature Sensor under different ODR_T

ODR (Hz)	4800	2400	1200	600	300	150	75	37.5	18.75	10	5
RMS Noise in ℃	0.0079	0.0060	0.0045	0.0038	0.0032	0.0020	0.0015	0.0011	0.0008	0.0008	0.0007

4.2.2. External temperature sensor

When external temperature sensor mode is selected, the temperature sensing signal input from the TEMP pin is buffered for TADC conversion. The reference voltage of the TADC is also VREF. The gain of the TADC can be 1X, 2X and 4X. The relationship between $TDATA_{RAW}$ and the temperature input is

$$TDATA_{RAW} = VTEMP * GAIN\_T / VREF * 2^{23}$$

When RAW_T = 0, the built-in MCU calibrated the offset, sensitivity and nonlinearity of the measured temperature signal. The external temperature sensing can be done in many ways, including NTC, RTD, diode and sensor bridge resistance itself. Figure 4.3 gives an example using a low TC drift resistor to sense the bridge resistance, which is usually proportional to the temperature of the sensor element. In case the bridge sensor is current driven, the bridge voltage can be used as temperature sensing input directly.

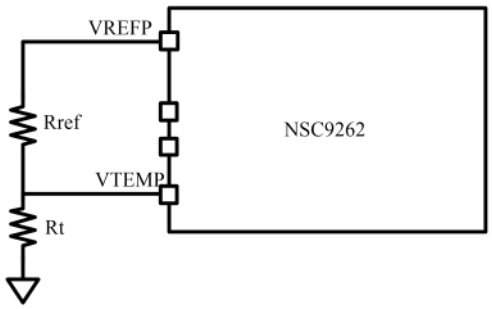


Figure 4.3 External temperature sensing using sensor bridge and a reference resistor

The output data rate of TADC can be set by 'ODR_T', similar as the primary signal channel. The relationship between ODR_T and the ENOB of TADC is shown in Table 4.3.

Table 4.3 ENOB of TADC under different ODR_T (External temperature sensor mode)

ODR_T(HZ)	ENOB		
	GAIN_T=1	GAIN_T =2	GAIN_T =4
4800	17.2	17.0	16.4
2400	17.6	17.4	16.7
1200	18.0	17.6	16.7
600	18.3	17.8	16.9
300	18.6	18.0	17.1
150	19.0	18.4	17.5
75	18.9	18.1	17.1
37．5	19.4	18.2	17.6
20	19.8	18.9	18.0
10	19.8	19.1	18.0

5	20.4	19.4	18.3

4.3. LIN INTERFACE MODULE

The LIN interface module includes LIN protocol control part and LIN physical transceiver part, as shown in Figure 4.4.

LIN protocol control part is used for frame structure in data link layer, node configuration in transport layer and data process of measuring channels in application layer. Meanwhile it supports diagnostic function of Class I. The integrated LIN transceiver part is compatible with LIN Specification 1.3//2.0/2.1/2.2, which reduces the external electronic components and simplify the complexity of sensor system.

An internal time-out filter prevents the LIN-bus from being permanently driven in dominant state. If TXD-signal is at low level for longer than $t_{TXDTIMEOUT}$, the pin LIN is switched off to recessive mode. To reset this mode the pin TXD has to be switched high.

An internal wake-up filter helps the chip to switch from low-power sleep mode to normal operation mode, with wake-up event of qualified pulse signals detected from LIN-bus.

For a detailed description, refer to the application note *NSC9262 LIN Interface Description*.

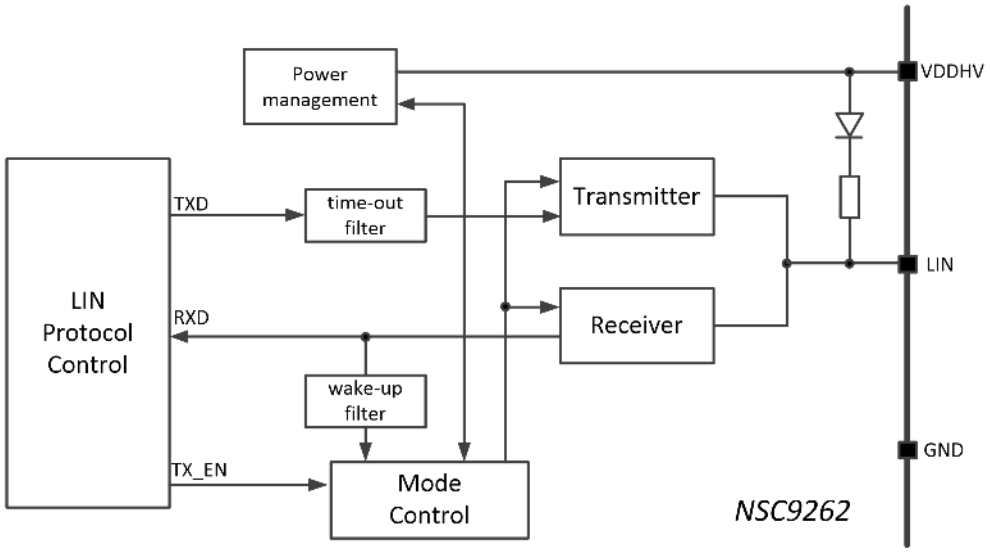


Figure 4.4 LIN interface module diagram

4.4. POWER MANAGEMENT

The NSC9262 internally includes a precision bandgap reference with very low temperature drift, less than 0.2% during full temperature range (-40~125˚C). This reference voltage is used in the constant voltage or current driving circuits for clock generator and ADC etc.

4.4.1. Power on Reset

A POR block is integrated in the NSC9262 for power on reset and EEPROM loading. When AVDD<2.5V, the chip is in reset state. After AVDD > 2.5V, the POR output is released and EEPROM is loaded afterwards. The POR circuits have 100mV hysteresis, that is to say the chip won't go into the reset state again until the AVDD is dropped as low as 2.4V.

4.4.2. Over-voltage and Reverse voltage Protection

The NSC9262 integrates an Over-voltage and Reverse voltage Protection on power supply. Over-voltage as high as 40V and Reverse voltage as low as -40V are allowed. In the case of Over-voltage, AVDD is clamped at a normal voltage as to protect the internal circuit.

4.5. BUILD-IN MCU CORE AND CONTROL LOGICS

4.5.1. Work Modes

Two Different work modes are supported by the NSC9262, command mode and active mode, which can be configured by the register 'CMD' (Reg0x30).

4.5.1.1. Command Mode

The command mode can be entered by writing the register 'CMD' with 0x00, which is used for configuring the chip outside. All the EEPROM registers can only be modified in this mode.

4.5.1.2. Active Mode

The active mode is the default mode after powering up, which can also be entered by writing the register 'CMD' with 0x03. In this mode, the primary measurement channel and the temperature channel continuously update their measured values into the 'PDATA' or 'TDATA' registers, and the selected output mode will be activated simultaneously. When the register bit 'RAW_P/T' = 1, the ADC conversion results will be put into the 'PDATA' or 'TDATA' directly, otherwise, every time the primary measurement channel ADC conversion ends, the build-in MCU core does once sensor calibration flow with the latest temperature value measured.

4.5.2. EEPROM

57 bytes EEPROM is contained in the NSC9262 to store the chip configurations and sensor calibration coefficients.

4.5.2.1. Loading

The contents of the EEPROM will be loaded into the EEPROM registers automatically after power up or soft-reset with the CRC checking. If the calculated CRC result does not match with what stored in the EEPROM, the 'CRC_ERROR' bit will be set and the analog output state will be decided according to the fault diagnostic and alarm configurations. Another status register bit 'LOADING_END' will be set after the loading completes.

4.5.2.2. Programming

Writing EEPROM registers will not program the EEPROM directly. The contents of the EEPROM registers will be programmed into the EEPROM by following sequence:

1. Set the register byte 'COMMAND' (Reg0x30) with 0x23 to enter EEPROM programming mode
2. Writing the register byte 'EE_PROG' (Reg0x6A) with 0x3E or 0xBE to start EEROM programming.

During EEPROM programming, a new CRC check code will be generated according to the contents of the EEPROM registers and will be programmed to the EEPROM simultaneously. The content of the 'EE_PROG' register will automatically come back to 0x00 to indicate the programming is done. A re-powering up or soft-reset is needed to reload the EEPROM contents back to the EEPROM registers to check the programmed value.

4.5.2.3. Lock and Unlock

The EEPROM inside the NSC9262 can be locked by setting the 'EEPROM_LOCK' bit and programming it into the EEPROM. After locked, the EEPROM cannot be programmed again, and only a special EVA-kits provided by NOVOSENSE can unlock it.

4.5.3. Build-in MCU Core

The NSC9262 is integrated with a built-in MCU core, which performs the signal processing, sensor calibration, EEPROM loading and programming etc. The MCU's program code is pre-stored in the internal ROM, which cannot be modified by customers. Please contact NOVOSENSE if a customized MCU program code is needed.

4.5.4. Calibration

The NSC9262 can compensate the sensor with offset, sensitivity, up to the 2^{nd} order offset temperature drift, up to the 2^{nd} order sensitivity temperature drift, up to the 3^{rd} order non-linearity, and the totally calibration error is less than 0.1% of the full span.

4.6. DIAGNOSTIC AND ALARM

NSC9262 can detect that the capacitor input pin is open, or there is leakage current at the capacitor input pin.

NSC9262 supports over-voltage detection and under-voltage detection. The over-voltage detection threshold is 35V and the under-voltage detection threshold is 6V.

NSC9262 supports temperature out-of-range check and thermal shutdown protection. The over temperature threshold is 180˚C. When thermal shut down happens, the output driver of LIN interface is off until the temperature recovers. NSC9262 records whether there is thermal shut down happens after recent power-on-reset.

Besides the sensor diagnostic functions, the NSC9262 supports ROM failure check, EEPROM CRC check, watch-dog timeout check, out-of-range detection of measuring channels and the error handling function for LIN protocol, including Response Error, Checksum Error and Bit Error.

Any of the above internal error detections has indicated a failure. The failure is annunciated through the status bits in the signal data for alarming.

5.0 SERIAL INTERFACE

The OWI serial interface is supported in the NSC9262 to configure registers, program EEPROM and poll measured data. When register bit 'OWI_DIS' = 0, the time between 5ms and 80ms after powering up is defined as the OWI access window. If a dedicated 24-bit OWI entering pattern is detected via OWI pin during this window, the chip enters OWI communication mode, otherwise enters LIN output mode (as shown in Figure 5.1).

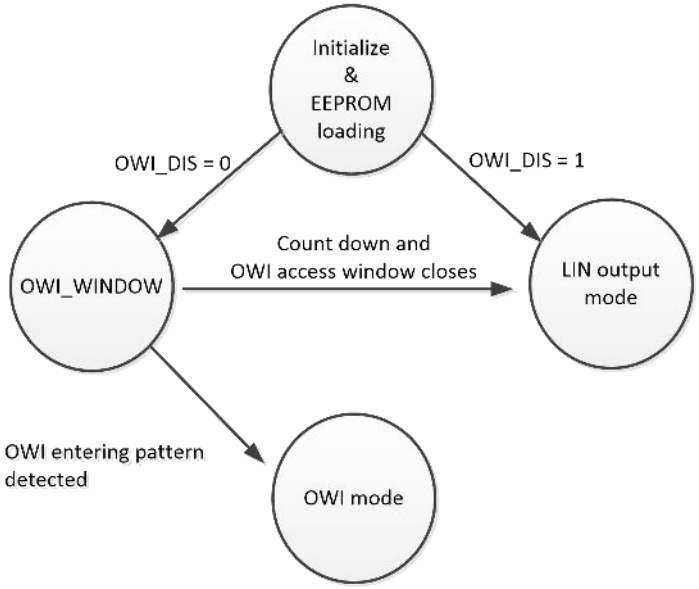


Figure 5.1 Definition of serial communication mode

5.1. OWI PIN CONFIGURATION

The OWI pin is shared with the LIN pin as open-drain output. An external pull-up resistor is needed for the OWI pin.

5.2. TIMING SPEC

Table5.1: OWI Timing Spec

Symbol	*Description*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*
t_{period}	OWI bit period		20		4000	Us
t_{pulse_0}	Duty cycle for 0		1/8	1/4	3/8	t_{period}
t_{pulse_1}	Duty cycle for 1		5/8	3/4	7/8	t_{period}
t_{start}	Start low pulse time		20		4000	Us
t_{stop}	Stop condition time		2			t_{period}

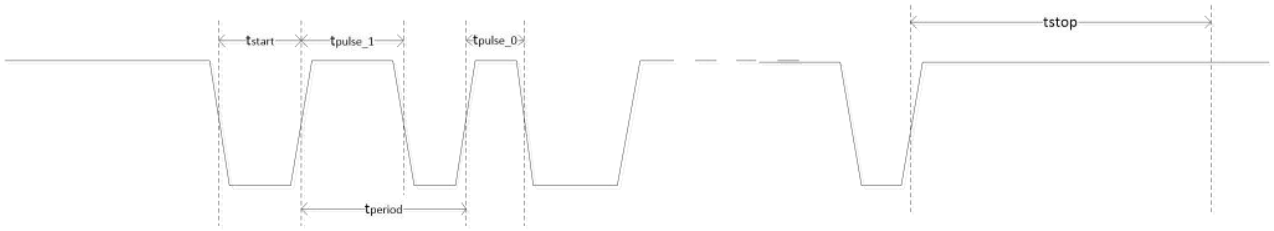


Figure 5.2 OWI Timing

5.3. ENTER OWI MODE

If 'OWI_DIS' = 0, the period between 5ms and 80ms after powering up is OWI access window. If a dedicated 24-bit OWI entering pattern (0xB5A6C9, as shown below) is detected via OWI pin during this window, the chip enters OWI communication mode. If 'OWI_DIS' = 1, there is no counting down for OWI window and the LIN output mode is directly access.

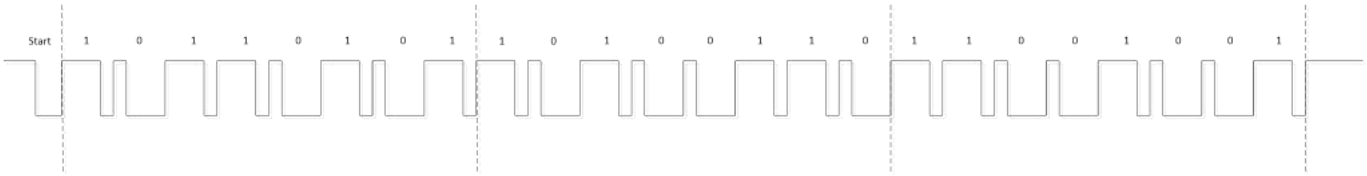


Figure 5.3 OWI Entering Pattern

During OWI communication, the bit period is determined by the period of the last bit of OWI entering pattern, and cannot be changed within the entire communication. So the bit period during OWI communication should be kept the same as the OWI entering pattern.

5.4. OWI PROTOCOL

The OWI protocol used is defined as follows:

a) Idle State

During inactivity of the bus, OWI line is pulled-up to high voltage level.

b) Start Condition

When OWI line is in idle state a low pulse (return to high) with a pulse width between 20us to 4ms indicates a start condition. Every command has to be initiated by a start condition sent by the master. The master can only generate the start condition when the OWI line is in idle state.

c) Stop Condition

After the write or read operation ends, the bus comes back to the idle state automatically. During any time of a transmission, the bus can be set back to the idle state by forcing the OWI line constant high or low voltage level for at least two times of the bit period (tBperiod)

d) Addressing

After the start condition, the master sends the addressing information, consisting of an 8-bit register address (MSB first), 2-bit byte number and a read/write–bit (0–write, 1–read). The register address indicates which register you will write into or read from; the byte number indicates how many bytes will write/read continuously: 00: 1byte, 01:2bytes, 10:3bytes, 11:4bytes; the read/write-bit indicates it a read operation (0) or write operation (1).

e) Write Operation

During transmission from master to slave (WRITE), the read/write bit is followed by 1/2/3/4 bytes (according to the byte NO. bits) transmitted data (MSB first), and the addressed register and follows will be refreshed to the written data after a stop condition.

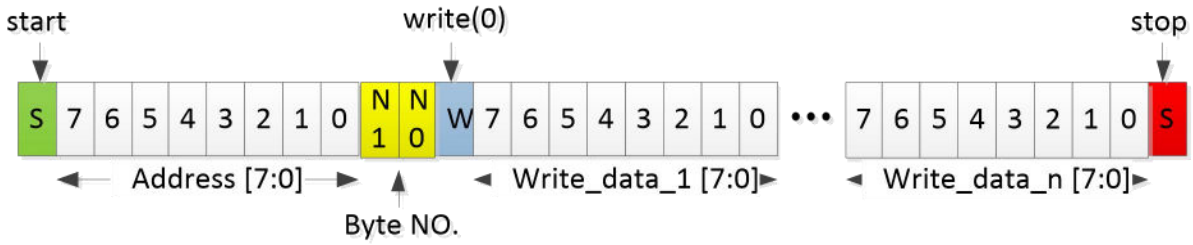


Figure 5.4 OWI Write Operation

f) Read Operation

During transmission from slave to master (READ), the master should set its OWI port as input after the read/write bit is sent, then the slave begins to transmit 1/2/3/4 bytes (according to the byte NO. bits) data (MSB first), which is contented in the addressed register and follows. Each data bytes include 8 bits of data and 2 bits of parity check code C1 and C0.

C1 = Read_data[7] ^ Read_data[5] ^ Read_data[3] ^ Read_data[1];

C0 = Read_data[6] ^ Read_data[4] ^ Read_data[2] ^ Read_data[0];

The master can check the transmission with the parity check code. After all data bytes transmitted, the slave goes back to idle state automatically.

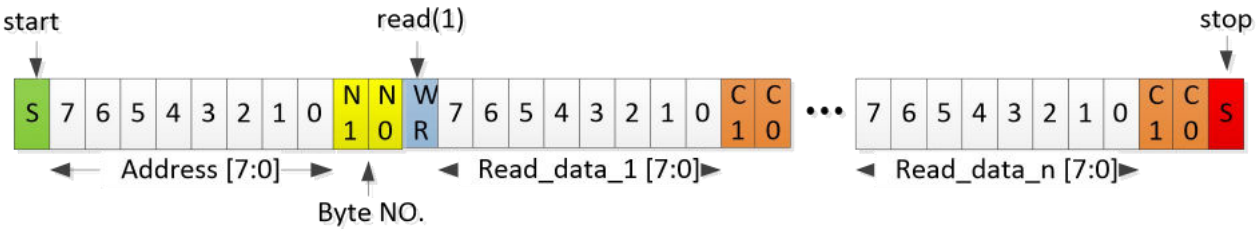


Figure 5.5 OWI Read Operation

5.5. QUIT OWI COMMUNICATION

Writing Reg0x61 with 0x5d during OWI mode results in quitting the OWI communication for LIN output.

6.0 PACKAGE INFORMATION

The NSC9262 uses SSOP16 package. The pin configuration is shown as below:

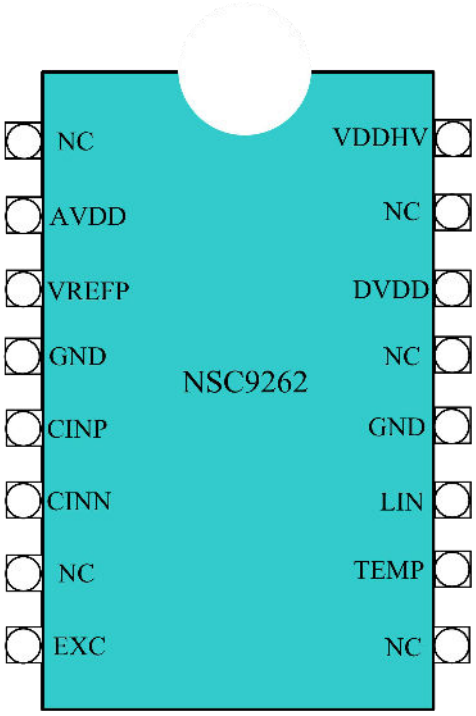
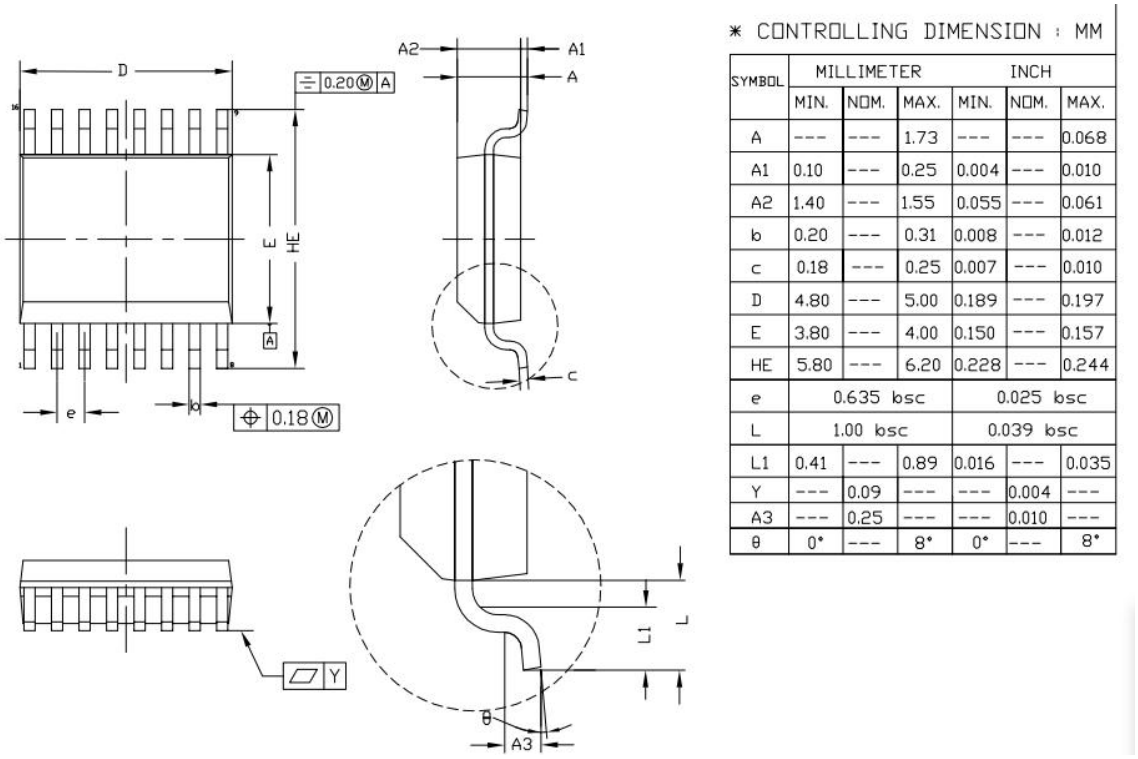


Figure 6.1 SSOP-16 package pin configuration



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.73	---	---	0.068
A1	0.10	---	0.25	0.004	---	0.010
A2	1.40	---	1.55	0.055	---	0.061
b	0.20	---	0.31	0.008	---	0.012
c	0.18	---	0.25	0.007	---	0.010
D	4.80	---	5.00	0.189	---	0.197
E	3.80	---	4.00	0.150	---	0.157
HE	5.80	---	6.20	0.228	---	0.244
e	0.635 bsc			0.025 bsc		
L	1.00 bsc			0.039 bsc		
L1	0.41	---	0.89	0.016	---	0.035
Y	---	0.09	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
θ	0°	---	8°	0°	---	8°

Figure 6.2 SSOP16Package Shape and Dimension

Table6.1 SSOP16 Pin Configuration and Description

SSOP16 Pin No.	Pin Name	Type	Description

1	NC	NC	Floating
2	AVDD	Supply	Internal Power Supply
3	VREFP	Analog	Reference Voltage Output/Input
4	GND	Supply	Ground
5	CINP	Analog	Capacitance measurement channel input positive
6	CINN	Analog	Capacitance measurement channel input negative
7	NC	NC	Floating
8	EXC	Analog	Output excitation source
9	NC	NC	Floating
10	TEMP	Analog	External temperature sensor input
11	LIN	Digital	LIN interface
12	GND	Supply	Ground
13	NC	NC	Floating
14	DVDD	Analog	1.8V DVDD digital LDO output
15	NC	NC	Floating
16	VDDHV	Supply	Power supply with OVP/RVP

7.0 ESD PROTECTION AND EMC SPECIFICATION

All pins have an ESD protection of >1500V according to Human Body Model(HBM). In addition, the VDDHV and LIN pin has an ESD protection of >8000V (system level).

The ESD test follows the Human Body Model with 1.5kOhm/100pF according to AEC-Q100-002 RevE. The system level ESD test of VDDHV and LIN pin follows the specification with 330Ω/330pF according to ISO 10605:2008(E).

About the detailed EMC performance, please refer to *NSC9262 Application Note.*

8.0 TYPICAL APPLICATIONS

8.1. APPLICATION 1

Capacitive sensor application circuit with LIN output is shown in Figure 8.1.

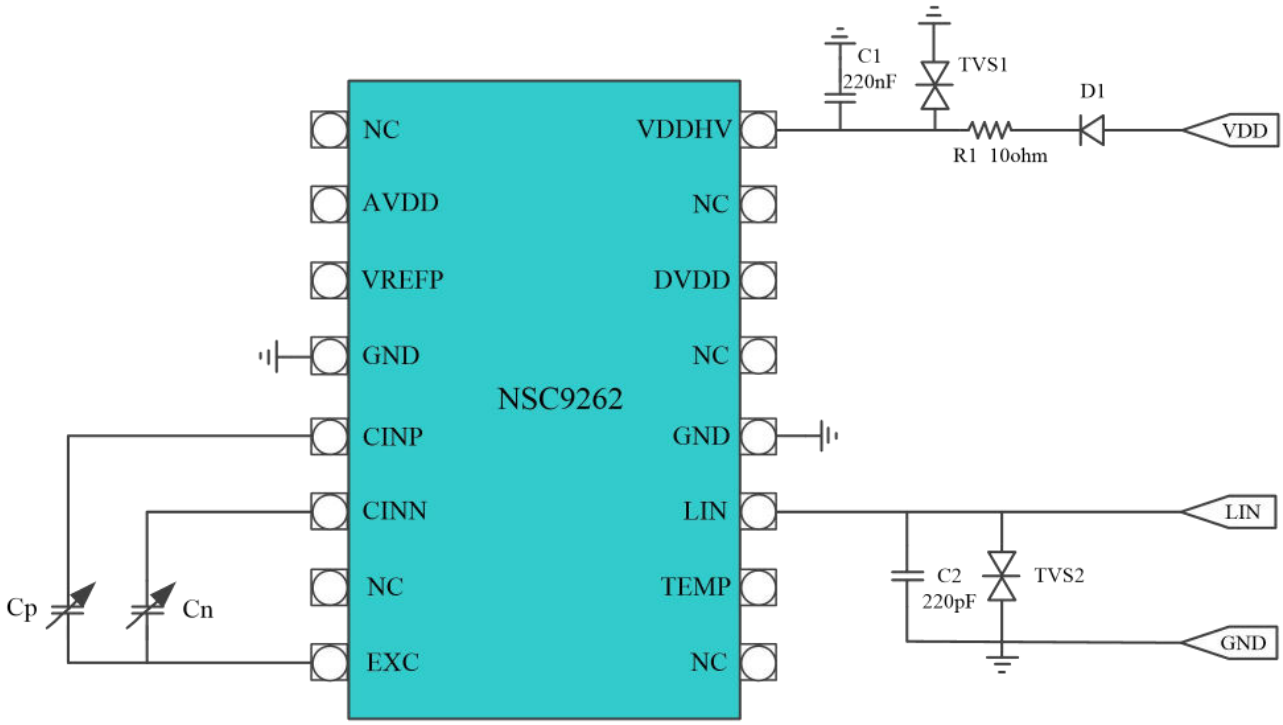


Figure 8.1 Capacitive Sensor with LIN output

9.0 TAPE/REEL INFORMATION

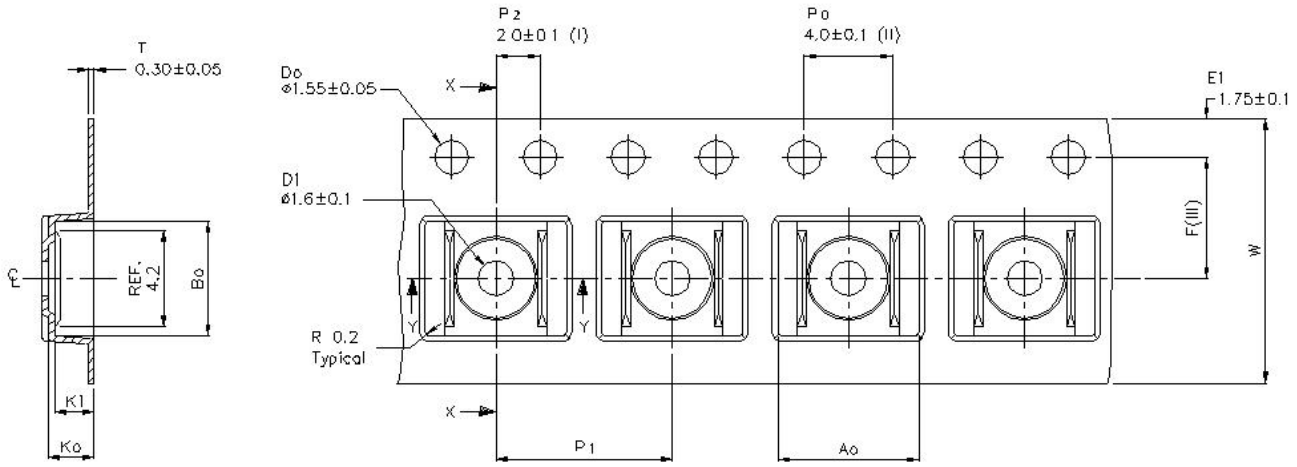
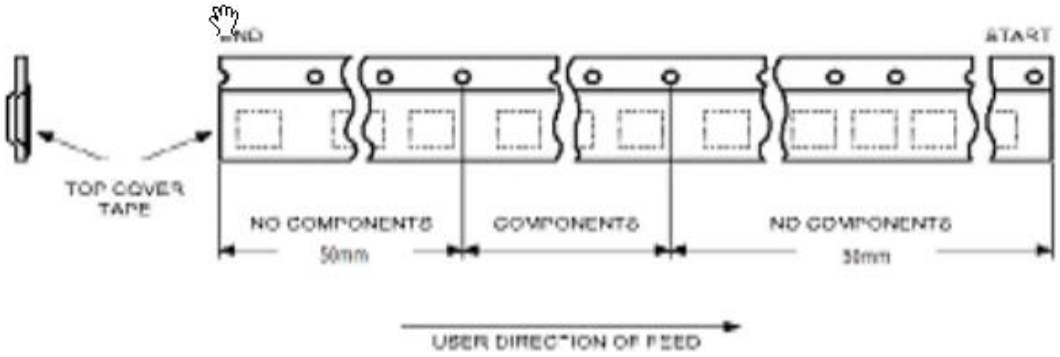


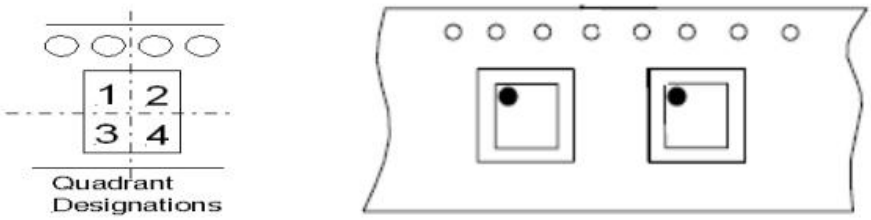
Figure 9.1 Tape/reel digram for SSOP16

Part No.	Package type	A0 (mm)	B0 (mm)	K0 (mm)	K1 (mm)	F (mm)	P1 (mm)	W (mm)
NSC9262-QSSR	SSOP16	6.5±0.1	5.3±0.1	2.2±0.1	1.9±0.1	5.5±0.1	8.0±0.1	12.0±0.3

There is no component at the head and the tail of each tape/reel, where the space is 50cm, as shown in the following figure.



Pin 1 is located at the first quadrant，as shown in the following figure.



10.0 ORDER INFORMATION

Part No.	Unit	Description
NSC9262-QSSR	2500ea/REEL	16-PIN SSOP16

11.0 RELATED DOCUMENTS

Document
NSC9262 Application Note
NSC9262 LIN Interface Description
NSC9262 Calibration Algorithm Introduction

12.0 REVISION HISTORY

Revision	Description	Date
0.0	Initial Version	2019/3/18
1.0	First Release	2019/12/13
1.1	Add ESD/EMC description Add list of related documents	2020/2/20
1.2	Add RoHS-compliant information Add document of Calibration Algorithm Introduction	2020/3/23