NSC2860X
General Capacitive Sensor Conditioner
Datasheet (EN) 1.0

Product Overview

The NSC2860X is an ASSP chip developed specifically for industrial transmitters with 4~20mA current output, 0~5V voltage output or 0~10V voltage output. It is designed to interface with capacitive pressure sensors by integrating an internal capacitance-to-voltage conversion circuit. It also provides a convenient OWI interface for direct communication via analog output line, allowing customers to easily calibrate and store calibration coefficients after sensor assembly. In addition, the NSC2860X also integrates a JFET controller that can be used directly in standard industrial loop power applications at 24V without the need for an additional power supply controller. This chip has been widely used in industrial capacitive pressure transmitter applications over the past few years, and its reliability and stability have been well proven by large shipments in the industrial field.

Key Features

- Integrated JEFT controller
- C/V converter with at most ±16pF differential input
- 24-bit ADC for primary signal measurement
- 24-bit ADC for temperature measurement
- Internal and external temperature sensor supported
- Low drift voltage reference
- 1x to 8x digital gain
- 16-bit DAC
- Multiple filter settings
- Built in sensor calibration logic
- 4～20mA output
- Ratio metric or absolute voltage output
- PWM output
- I2C, SPI, OWI output
- 64 Bytes EEPROM
- Operation temperature: -40℃~125℃

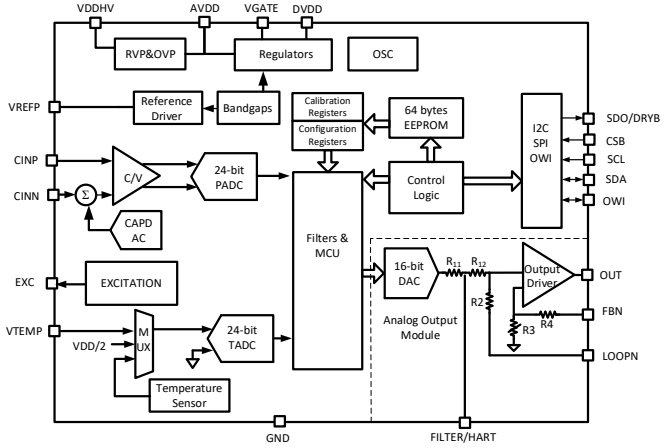
Applications

- Capacitive pressure sensors and transmitters

Device Information

Part Number	*Package*	*Body Size*
NSC2860X	QFN20	4mm × 4mm

Functional Block Diagrams



NSC2860X Block Diagram

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1. Pin Configuration and Functions

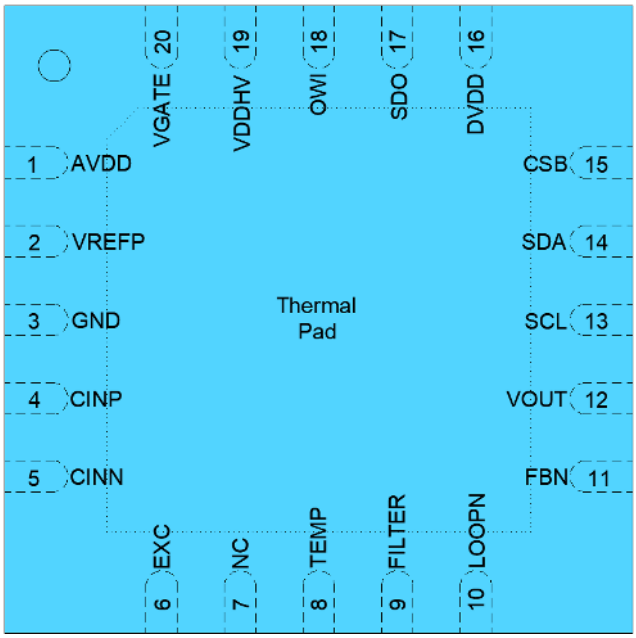


Figure 1.1 NSC2860X Package

Table 1.1 NSC2860X Pin Configuration and Description

NSC2860X PIN NO.	*SYMBOL*	*FUNCTION*
1	AVDD	Power Supply
2	VREFP	Reference Voltage Output/Input
3	GND	Ground
4	CINP	Analog input positive
5	CINN	Analog input negative
6	EXC	Excitation source
7	NC	**Must be left floating**
8	TEMP	External temperature sensor input (ODR_T≠1111b) External Negative Reference Voltage input (ODR_T=1111b)
9	FILTER	DAC output filter capacitor / HART signal coupling terminal
10	LOOPN	Negative loop line for 4~20 mA application
11	FBN	External feedback pin
12	VOUT	Analog output

13	SCL	I2C/SPI clock signal
14	SDA	I2C data signal (SDA) or SPI data signal (SDIO)
15	CSB	I2C/SPI mode selection pin, SPI chip selection
16	DVDD	1.8V DVDD digital LDO output
17	SDO	4-wire SPI date output
18	OWI	One-wire interface
19	VDDHV	Power supply with OVP/RVP
20	VGATE	JFET regulation output

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDDHV	-24		28	V	70℃, 1 hour
	AVDD	-0.3		6.5	V	
VGATE Voltage	VGATE	-0.3		7.5	V	
LOOPN Voltage	LOOPN	-1.2		0.3	V	
Analog pin voltage		-0.3		AVDD+0.3	V	
Analog pin current Limit				25	mA	
Digital pin voltage		-0.3		AVDD+0.3	V	
Maximum junction temperature	Tjmax			155	℃	
Operating Temperature	Topr	-40		85	℃	Best performance temperature range.
		-40		125	℃	Normal temperature range.
Storage Temperature	Tstg	-60		150	℃	
Electrostatic discharge	HBM		±2000		V	
	CDM		±500		V	

3. Electrical Characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDDHV	3	5	5.5	V	
JFET Regulator Output	VDDJ	4.9	5	5.2	V	JFET_LVL=0
		3.2	3.3	3.5	V	JFET_LVL=1

	PSRR		100		dB	@DC
			40		dB	@20kHz
DVDD Output Voltage	DVDD	1.7	1.78	1.85	V	
Power On Reset	V_{POR_AVDD}		2.5		V	POR threshold as power up
	V_{POR_HYS}		0.1		V	POR Hysteresis
Operating Current (Sensor not included)	I_{DD1}		1.6		mA	Current output mode (OUT_MODE=01xb)
	I_{DD2}		1.55		mA	Voltage output mode (OUT_MODE=00xb)
	I_{DD3}		1.4		mA	Digital mode (OUT_MODE=111b)
	I_{CMD}		115		uA	Command mode SPI/I2C mode, JFET_DIS=1
Reference Voltage and Current Source						
Internal Bandgap Reference	VBG		1.200		V	Not measurable directly, proportional with VREF.
VBG TC	VBG_TC		5	25	ppm/℃	-40°C~105℃
			5	30	ppm/℃	-40°C~125℃
VREF Output	VREF		2		V	
Load on VREF	RVREF	0.5			kohm	
VREF Current Limit	I_{VREF_limit}		20		mA	Short to Ground
Primary Signal Measurement Channel						
Differential Input Capacitance Range	C_{RANGE} CV_Gain=0		±16		pF	CV_RANGE<1:0>=2'b00
			±12		pF	CV_RANGE<1:0>=2'b01
			±8		pF	CV_RANGE<1:0>=2'b10
			±4		pF	CV_RANGE<1:0>=2'b11
	C_{RANGE} CV_Gain=1		±8		pF	CV_RANGE<1:0>=2'b00
			±6		pF	CV_RANGE<1:0>=2'b01
			±4		pF	CV_RANGE<1:0>=2'b10
			±2		pF	CV_RANGE<1:0>=2'b11
Common Mode Capacitance Range	C_{CM_RANGE}		48		pF	CV_RANGE<1:0>=2'b00
			36		pF	CV_RANGE<1:0>=2'b01
			24		pF	CV_RANGE<1:0>=2'b10
			24		pF	CV_RANGE<1:0>=2'b11

CAPDAC Range		0		63.5	pF	Register setting, 0.5pF/LSB
PADC Resolution	RES_P		24		Bits	
PADC Output Data Rate	ODR_P	2.5		2400	Hz	
ENOB of Primary Channel	ENOB_P	Refer to Table5.1			Bits	Depends on C_{RANGE} and ODR_P
Excitation Source (EXC)						
Excitation Frequency	CV_FREQ		38.4		kHz	CV_RANGE<1:0>=2'b00/01
			76.8		kHz	CV_RANGE<1:0>=2'b10/11
Excitation Voltage Amplitude	VAC		2		V	
Drivability	DRV		50		pF	
Temperature Measurement Channel (Internal and External Temperature Sensor)						
TADC Resolution	RES_T	24			Bits	
TADC GAIN	GAIN_T	1		4		1,2,4
TADC Output Data Rate	ODR_T	2.5		2400	Hz	
TADC ENOB	ENOB_P	Refer to Table 5.2				
Error of Internal Temperature Sensor			±1.5	±3	℃	-40 to 125 ℃
TEMP Input Impedance			1		Gohm	
Voltage Output						
DAC Output Full Scale	VFS	5V, 3.3V, 1.2V or Ratio-metric				Depends on DAC_REF<1:0>
DAC Output RMS Noise	V_{RMS}		0.5		mV	
Output Load Resistance	R_{LOAD}	1			kohm	PGA off, Buffer off
Output Load Capacitance	C_{LOAD}			150	nF	
Output Shorted Current	I_{LIMIT}		20		mA	
Clamp High Level	V_{clampH}	0.5		1	VFS	Set by CLAMP_HIGH<7:0>
Clamp Low Level	V_{clampL}	0		0.5	VFS	Set by CLAMP_LOW<7:0>
4~20 mA Output						
Loop Reference Resistor	R_{LOOP}		50		ohm	
Current RMS Noise	I_{RMS}		0.2		uA	0.1~10Hz
OSC						
ADC Clock	F_{OSC_MOD}		614.4		kHz	
Clock Rate Error	F_{OSC_ERR}	-2%		1%		-40~125℃
PDM/PWM						
PDM Modulation Frequency	F_{PDM}	19.2		153.6	kHz	

PWM Frequency	F_{PWM}		300		Hz	
PWM Resolution			12		Bits	
EEPROM						
Programming Temperature	TEEP	-40		105	℃	
Programming Supply Voltage	VEE	3		5.5	V	
Time for EEPROM programming	t_{EEP}		0.8	1	s	
Endurance			1000		Cycle	
Date Retention		10			Year	@150℃
Serial Interface						
Communication Data Rate	Fsclk			10	MHz	SPI Interface
				400	kHz	I2C Interface
				50	kHz	OWI Interface

4. Register Description

The register map of the NSC2860X includes two parts, normal registers and EEPROM registers. The normal registers include data registers and some control registers, while the EEPROM registers are mainly configuration registers and calibration coefficients. All EEPROM registers should be written by external interface on command mode (register 'CMD' = '0x00').

4.1. Normal Registers

IF_CTRL(R/W)

Address	Bit	Register name	Default	Description
0x00	7，0	SDO_ACTIVE	1'b1	0: SPI3-wire. 1: SPI4-wire (SDO as serial output).
	6，1	LSB_FIRST	1'b0	0: SPI MSB first. 1: SPI LSB first.
	5, 2	SOFTRESET	1'b0	Set either of these two bits to 1 to reset the chip. Return to 0 after reset.

STATUS (Read only)

Address	Bit	Register name	Default	Description
0x02	7 – 3	Reserved	5'b00000	Reserved
	2	CRC_ERR	1'b0	1: CRC error detected during EEPROM loading. When CRC error is asserted, EEPROM register bits 'OWI_DIS', 'OWI_AC_EN', 'OWI_WINDOW', 'JFET_DIS', 'VREF_DIS', 'EEPROM_LOCK' are forced to 0.
	1	LOADING_END	1'b0	1: EEPROM loading end flag.
	0	DRDY	1'b0	1: Set after a new data updated and automatically cleared after a register reading to PDATA/TDATA or before the next data's coming.

PDATA (Read only, Primary channel data register)

Address	Bit	Register name	Default	Description
0x06	7 – 0	PDATA<23:16>	0x00	Signed, 2's complement: When 'RAW_P= 1, stores the ADC output of primary channel, When 'RAW_P'=0, stores the calibrated primary channel data.
0x07	7 – 0	PDATA<15:8>	0x00	
0x08	7 – 0	PDATA<7:0>	0x00	

TDATA (Read only, temperature channel data register)

Address	Bit	Register name	Default	Description
0x09	7 – 0	TDATA<23:16>	0x00	Signed, 2's complement: When 'RAW_T' = 1, stores the ADC output of temperature channel, When 'RAW_T'= 0, stores the calibrated temperature data, LSB = 1/2^16 ℃. Real Temperature =TDATA/2^16+25 ℃
0x0a	7 – 0	TDATA<15:8>	0x00	
0x0b	7 – 0	TDATA<7:0>	0x00	

COMMAND (R/W, command register)

Address	Bit	Register name	Default	Description
0x30	7 – 0	CMD<7:0>	0x03	0x00: command mode, all EEPROM registers can be written only in command mode. 0x01/0x02: Single mode. 0x03: Continuous mode. 0x33: EEPROM program mode.

QUIT_OWI (Write only)

Address	Bit	Register name	Default	Description
0x61	7 – 0	QUIT_OWI <7:0>	0x00	Write'0x5D' to this register to quit OWI communication. If 'QUIT_OWI_CNT' =0x00, quit OWI communication permanently. If 'QUIT_OWI_CNT' is not 0x00, quit OWI mode temporary with a certain time and then get back to OWI mode.

QUIT_OWI_CNT (R/W)

Address	Bit	Register name	Default	Description
0x62	7 – 0	QUIT_OWI_CNT <7:0>	0x00	Time for temporary quit OWI communication Mode. 0x00： Quit forever, 0x01： 50ms, 0x02： 100ms … 0xFF： 12.8s

EE_PROG (R/W)

Address	Bit	Register name	Default	Description
0x6a	7 – 0	EE_PROG<7:0>	0x00	Write '0x7E' or '0xFE' to start EEPROM programming. Automatically cleared to '0x00' after programming finished.

VDD_CHECK (R/W)

Address	Bit	Register name	Default	Description
0x70	0	VDD_CHECK	1'b0	Write '1' to force VDD/2 as the input of temperature ADC.

4.1. EEPROM Registers

SYS_CONFIG1 (R/W)

Address	Bit	Register name	Default	Description
0xa1	7	CAL_MODE	1'b0	0: one segment calibration with the 2nd order temperature coefficients 1: two segment calibration with the 1st order temperature coefficients.
	6-4	Reserved	3'b000	Reserved
	3	OWI_AC_EN	1'b0	0: Single-port OWI communication mode. 1: Dual-port OWI communication mode.
	2	OWI_WINDOW	1'b0	0: OWI can be entered during a 2.5ms~20ms window after power up or soft reset. 1: infinite window, OWI can be entered any time after power up.
	1	OWI_DIS	1'b0	1. OWI disabled (Won't be effective until next power on reset or

				soft reset after EEPROM is programmed).
	0	INT_EN	1'b0	1: Enable data ready interrupt, low level active.

SYS_CONFIG2 (R/W)

Address	Bit	Register name	Default	Description
0xa2	7	JFET_DIS	1'b1	1: Disable JFET regulation.
	6	JFET_LVL	1'b0	JFET_LVL=0: JFET output 5V. JFET_LVL=1: JFET output 3.3V.
	5	VREF_DIS	1'b0	1: Disable reference buffer and reference voltage can be forced externally.
	4	Reserved	1'b0	Reserved
	3	T_OUT_EN	1'b0	1: when not in OWI mode, TADC data outputs through OWI pin in PWM format.
	2 - 0	OUT_MODE<2:0>	3'b001	000: Voltage output with external feedback 001: Voltage output with internal feedback 010/011: Current output 100: PDM output 101: PWM output 111: DAC disabled

CV_CONFIG (R/W)

Address	Bit	Register name	Default	Description
0xa3	7	CV_MODE	1'b0	0: Drive mode for C/V converter 1: Ground mode for C/V converter
	6 – 0	CAPOFF<6:0>	0x00	Set internal CAPDAC offset for input CAPOFF = CAPOFF<6:0>*0.5pF

PCH_Config1(R/W)

Address	Bit	Register name	Default	Description
0xa4	7 – 4	CV_Gain	1'b0	If enabled, CV gain is double, in other words CRANGE is half.
	6	Reserved	1'b0	Reserved
	5 – 4	CV_RANGE<1:0>	2'b00	If CV_Gain=0: 00: CRANGE = ±16pF, CCM_RANGE = 48pF. 01: CRANGE = ±12pF, CCM_RANGE = 32pF. 10: CRANGE = ±8pF, CCM_RANGE = 24pF. 11: CRANGE = ±4pF, CCM_RANGE = 24pF. If CV_Gain=1: 00: CRANGE = ±8pF, CCM_RANGE = 48pF. 01: CRANGE = ±6pF, CCM_RANGE = 32pF. 10: CRANGE = ±4pF, CCM_RANGE = 24pF. 11: CRANGE = ±2pF, CCM_RANGE = 24pF.

	3 – 0	ODR_P<3:0>	4'b0000	PADC output data rate setting 0000:2.4kHz, 0001: 1.2kHz, 0010: 600Hz, 0011: 300Hz, 0100: 150Hz, 0101:75Hz, 0110:37.5Hz, 0111:18.75Hz, 1000:10Hz (with 60Hz notch), 1001:10Hz (with 50Hz notch), 1010:5Hz (with 60Hz notch), 1011:5Hz (with 50Hz notch), 1100:2. 5Hz (with 60Hz notch), 1101：2.5Hz (with 50Hz notch) 1110,1111: PADC disabled.

PCH_Config2(R/W)

Address	Bit	Register name	Default	Description
0xa5	7 – 6	DAC_REF<1:0>	2'b00	DAC full scale reference 00: 5V, 01: 3.3V, 10: 1.2V, 11: AVDD (ratio-metric)
	5 – 1	RESERVED	5'b00000	Reserved.
	0	RAW_P	1'b0	0: update calibrated sensor data into 'PDATA' register. 1: update raw PADC data into 'PDATA' register after conversion.

TCH_Config(R/W)

Address	Bit	Register name	Default	Description
0xa6	7	EXT_TEMP	1'b0	0: internal temperature sensor selected. 1: external temperature sensor selected (TEMP pin as external temperature sensor input).
	6 – 5	GAIN_T<1:0>	2'b00	Gain for temperature channel. 00:1X, 01:2X, 10/10:4X
	4 – 1	ODR_T	4'b0000	TADC output data rate, similar as ODR_P. 0000:2.4kHz, 0001: 1.2kHz, 0010: 600Hz, 0011: 300Hz, 0100: 150Hz, 0101:75Hz, 0110:37.5Hz, 0111:18.75Hz, 1000:10Hz (with 60Hz notch), 1001:10Hz (with 50Hz notch), 1010:5Hz (with 60Hz notch), 1011:5Hz (with 50Hz notch), 1100:2. 5Hz (with 60Hz notch), 1101：2.5Hz (with 50Hz notch) 1110,1111: TADC disabled.
	0	RAW_T	1'b0	1: store the raw TADC output into 'TDATA' register. 0: store the calibrated TADC data into 'TDATA' register.

CLAMPH(R/W)

Address	Bit	Register name	Default	Description
0xa7	7 – 0	CLAMPH<7:0>	0x00	Set clamping high level. (1- CLAMPH *2^(-9))* VFSDAC

CLAMPL(R/W)

Address	Bit	Register name	Default	Description
0xa8	7 – 0	CLAMPL<7:0>	0x00	Set clamping low level, CLAMPL *2^(-9) * VFSDAC

OFFSET0(R/W)

Address	Bit	Register name	Default	Description
0xa9	7 – 0	OFF0<15:8>	0x00	Sensor Calibration coefficient, offset at T0. LSB=1/2^15. Range (-1, +1).
0xaa	7 – 0	OFF0<7:0>	0x00	

CTC1(R/W)

Address	Bit	Register name	Default	Description
0xab	7 – 0	CTC1<15:8>	0x00	Sensor Calibration coefficient. CAL_MODE=0: the 1st order temperature coefficient of offset. LSB=1/2^22. Range (-0.00781, +0.00781). CAL_MODE=1: the 1st order temperature coefficient of offset for segment 0.LSB=1/2^22. Range (-0.00781, +0.00781).
0xac	7 – 0	CTC1<7:0>	0x00	

CTC2(R/W)

Address	Bit	Register name	Default	Description
0xad	7 – 0	CTC2<15:8>	0x00	Sensor Calibration coefficient. CAL_MODE=0: the 2nd order temperature coefficient of offset. LSB=1/2^29, Range (-6.1e-5, 6.1e-5). CAL_MODE=1: the 1st order temperature coefficient of offset for segment 1, LSB=1/2^22. Range (-0.00781, +0.00781).
0xae	7 – 0	CTC2<7:0>	0x00	

S0(R/W)

Address	Bit	Register name	Default	Description
0xaf	7 – 0	S0<15:8>	0x00	Sensor calibration coefficient, sensitivity at T0. LSB=1/2^15 (unsigned). Range (0, 2).
0xb0	7 – 0	S0<7:0>	0x00	

STC1(R/W)

Address	Bit	Register name	Default	Description
0xb1	7 – 0	STC1<15:8>	0x00	Sensor Calibration coefficient. CAL_MODE=0: the 1st order temperature coefficient of sensitivity. LSB=1/2^22. Range (-0.00781, +0.00781). CAL_MODE=1: the 1st order temperature coefficient of sensitivity for segment 0. LSB=1/2^22. Range (-0.00781, +0.00781).
0xb2	7 – 0	STC1<7:0>	0x00	

STC2(R/W)

Address	Bit	Register name	Default	Description
0xb3	7 – 0	STC2<15:8>	0x00	Sensor Calibration coefficient. CAL_MODE=0: the 2nd order temperature coefficient of sensitivity. LSB=1/2^29, Range (-6.1e-5, 6.1e-5). CAL_MODE=1: the 1st order temperature coefficient of sensitivity for segment 1, LSB=1/2^22. Range (-0.00781, +0.00781).
0xb4	7 – 0	STC2<7:0>	0x00	

KS(R/W)

Address	Bit	Register name	Default	Description
0xb5	7 – 0	KS<15:8>	0x00	Sensor calibration coefficient, the 2nd order nonlinearity coefficient. LSB=1/2^15. Range (-1, +1).
0xb6	7 – 0	KS<7:0>	0x00	

KSS(R/W)

Address	Bit	Register name	Default	Description

0xb7	7 – 0	KSS<15:8>	0x00	Sensor calibration coefficient, the 3rd order nonlinearity coefficient. LSB=1/2^16. Range (-0.5, +0.5).
0xb8	7 – 0	KSS<7:0>	0x00	

SCALE_OFF(R/W)

Address	Bit	Register name	Default	Description
0xb9	7 – 0	SCALE_OFF<23:16>	0xC0	SCALE offset coefficient. LSB=1/2^23. Range (-1, +1).
0xba	7 – 0	SCALE_OFF<15:8>	0x00	
0xbb	7 – 0	SCALE_OFF<7:0>	0x00	

SCALE_S(R/W)

Address	Bit	Register name	Default	Description
0xbc	7 – 0	SCALE_S<23:16>	0x01	SCALE sensitivity coefficient(unsigned). LSB=1/2^16 (unsigned), Range (0, 256).
0xbd	7 – 0	SCALE_S<15:8>	0x00	
0xbe	7 – 0	SCALE_S<7:0>	0x00	

T0(R/W)

Address	Bit	Register name	Default	Description
0xbf	7 – 0	T0<7:0>	0x00	Sensor calibration coefficient, reference temperature point. Real reference temperature: REAL_T0 = T0 + 25. LSB=1. Range (-128, +127).

KTS(R/W)

Address	Bit	Register name	Default	Description
0xc0	7 – 0	KTS<7:0>	0x00	Sensor calibration coefficient, the 2nd order nonlinearity coefficient for external temperature sensor. LSB=1/2^7. Range (-1, +1).

MTO(R/W)

Address	Bit	Register name	Default	Description
0xc1	7 – 0	MTO<15:8>	0x00	Sensor calibration coefficient, offset coefficient of external temperature sensor. LSB=1/2^15. Range (-1, +1).
0xc2	7 – 0	MTO<7:0>	0x00	

KT(R/W)

Address	Bit	Register name	Default	Description
0xc3	7 – 0	KT<15:8>	0x00	Sensor calibration coefficient, sensitivity coefficient of external temperature sensor. LSB=1/2^12. Range (-8, +8).
0xc4	7 – 0	KT<7:0>	0x00	

DAC_OFF(R/W)

Address	Bit	Register name	Default	Description
0xc5	7 – 0	DAC_OFF<15:8>	0x00	DAC calibration coefficient: DAC offset. LSB = 1/2^15. Range (-1, 1).
0xc6	7 – 0	DAC_OFF<7:0>	0x00	

DAC_GAIN(R/W)

Address	Bit	Register name	Default	Description
0xc7	7 – 0	DAC_GAIN<15:8>	0x00	DAC calibration coefficient: DAC gain. LSB = 1/2^16. Range (-0.5, 0.5).
0xc8	7 – 0	DAC_GAIN<7:0>	0x00	

PADC_OFF(R/W)

Address	Bit	Register name	Default	Description
0xc9	7 – 0	PADC_OFF<23:16>	0x00	PADC calibration offset coefficient. LSB=1/2^23. Range (-1, +1).
0xca	7 – 0	PADC_OFF<15:8>	0x00	
0xcb	7 – 0	PADC_OFF<7:0>	0x00	

PADC_GAIN(R/W)

Address	Bit	Register name	Default	Description
0xcc	7 – 0	PADC_GAIN<15:8>	0x00	PADC calibration gain coefficient. LSB=1/2^16. Range (-0.5, +0.5).
0xcd	7 – 0	PADC_GAIN<7:0>	0x00	

P0(R/W)

Address	Bit	Register name	Default	Description
0xce	7 – 0	P0 <7:0>	0x00	Sensor calibration coefficient, reference pressure point for nonlinearity calibration. LSB=1/2^7. Range (-1, 1).

SPARE(R/W)

Address	Bit	Register name	Default	Description
0xcf	7 – 0	Spare1<7:0>	0x00	User defined.
0xd0	7 – 0	Spare2<7:0>	0x00	
0xd1	7 – 0	Spare3<7:0>	0x00	
0xd2	7 – 0	Spare4<7:0>	0x00	
0xd3	7 – 0	Spare5<7:0>	0x00	
0xd4	7 – 0	Spare6<7:0>	0x00	
0xd5	7 – 0	Spare7<7:0>	0x00	
0xd6	7 – 0	Spare8<7:0>	0x00	

DIG_GAIN(R/W)

Address	Bit	Register name	Default	Description
0xd7	7–6	DIG_GAIN<1:0>	2'b00	Digital Gain Setting 00:1X, 01:2X, 10:4X, 11:8X
	5–0	Reserved	6b000000	Reserved.

RESERVED

Address	Bit	Register name	Default	Description
0xd8	7-0	Reserved	-	For NOVOSENSE INFO

EEPROM_LOCK(R/W)

Address	Bit	Register name	Default	Description
0xd9	7	EEPROM_LOCK	1'b0	1: EEPROM lock, set 1 and then EEPROM can't be programmed. (Won't be effective until next power on reset or soft reset after EEPROM is programmed)
	6 – 0	PARTID (read only)	7'b0000 011	NOVOSENSE chip ID

5. Function Description

5.1. Overview

The NSC2860X is a highly integrated capacitive sensor conditioner for industrial application. The chip supports over-voltage and reverse voltage protection. Current output, voltage output output and PDW/PWM output are all available. The NSC2860X uses differential inputs with at most ±16pF differential input capacitance range and 48pF common mode capacitance range. The chip incorporates five parts: analog front-end module, digital module, analog output module, power supply module and serial interfaces. The block diagram of the NSC2860X is shown in Figure 5.1.

Analog front-end module includes a primary signal measurement channel with a C/V converter followed by a 24-bit ∑Δ ADC, a temperature measurement channel with also a 24-bit ∑Δ ADC, for precision sensor signal and temperature measurement.

The digital module is composed of registers, EEPROM, control logic, and a built-in MCU. The sensor calibration algorithm is implemented with the built-in MCU and can supports up to 2nd order temperature drift compensation of offset and sensitivity for the sensor. It can also compensate the nonlinearity of sensor output up to 3rd order. The configuration parameters and coefficients for calibration are stored at in the EERPOM of 64 bytes.

The analog output module includes a 16-bit DAC and a flexible configurable output driver which can be configured to support analog output with several types of full scale range and PWM output.

The power supply module includes a high precision voltage reference, a sensor voltage driver, over-voltage and reverse voltage protection block and JFET controller.

The NSC2860X supports OWI serial interface, writing and reading registers of configuration, calibration coefficients and data. Through the highly integrated and flexible interface, the NSC2860X only needs one wire to realize sensor calibration, field verification and full scale range modification.

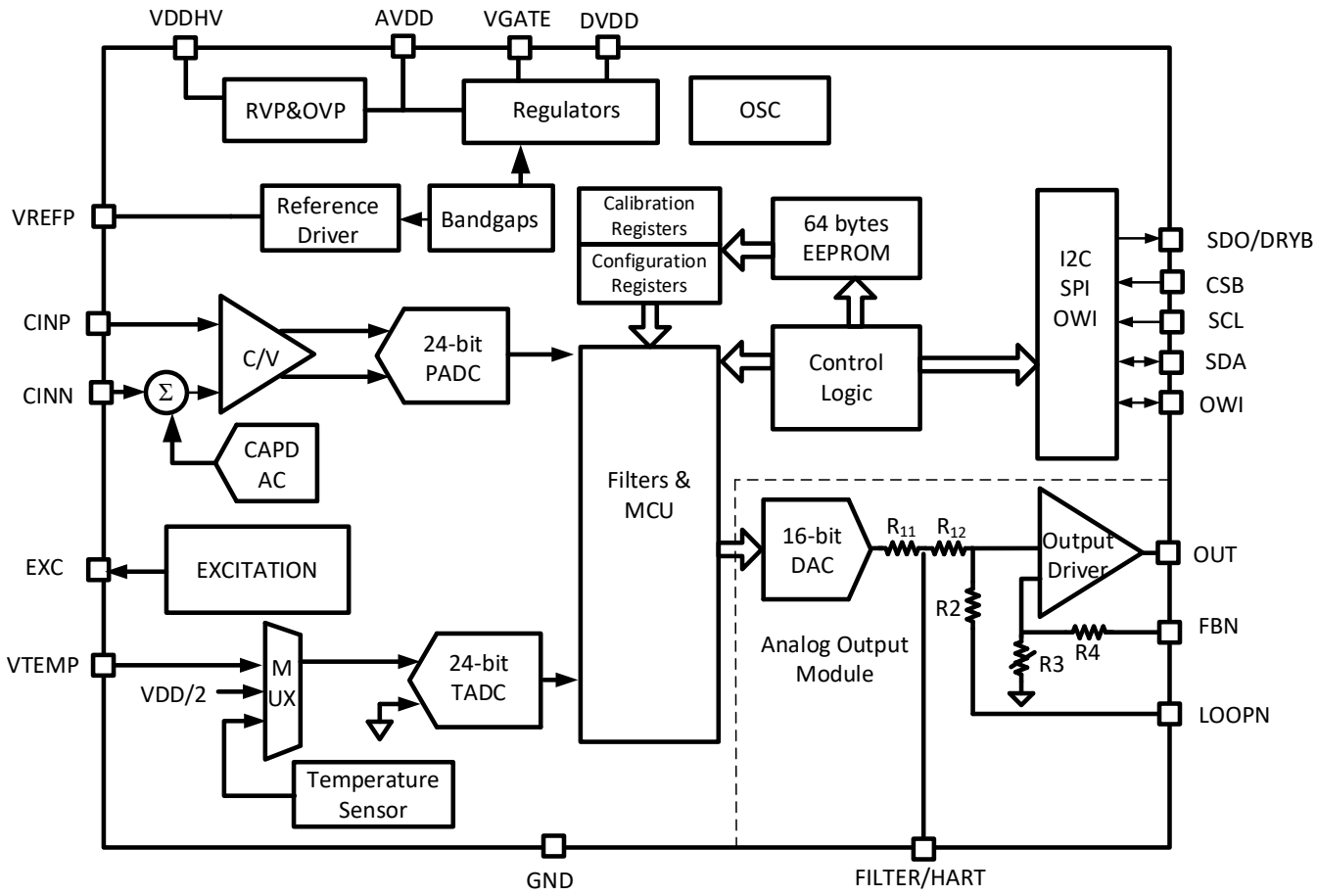


Figure 5.1 Block diagram of the NSC2860X

5.2. Analog Front-end Module 1: Primary signal channel

5.2.1. Capacitance measurement mode

The NSC2860X supports two types of capacitance measurement modes: Drive Mode and Ground Mode. The NSC2860X generates a square wave at EXC pin with 38.4KHz or 76.8KHz frequency and VREF amplitude, which is used to drive input capacitor at Drive Mode or shield parasitic capacitor at Ground Mode.

When CV_MODE = 0, the NSC2860X is at Drive Mode, where the external input capacitors are connected as shown in Figure 5.2. The differential input capacitors' common plate is driven by the square wave at EXC pin at Drive Mode. Since the voltage at CINP and CINN keep constant, the input parasitic capacitance would not affect the output.

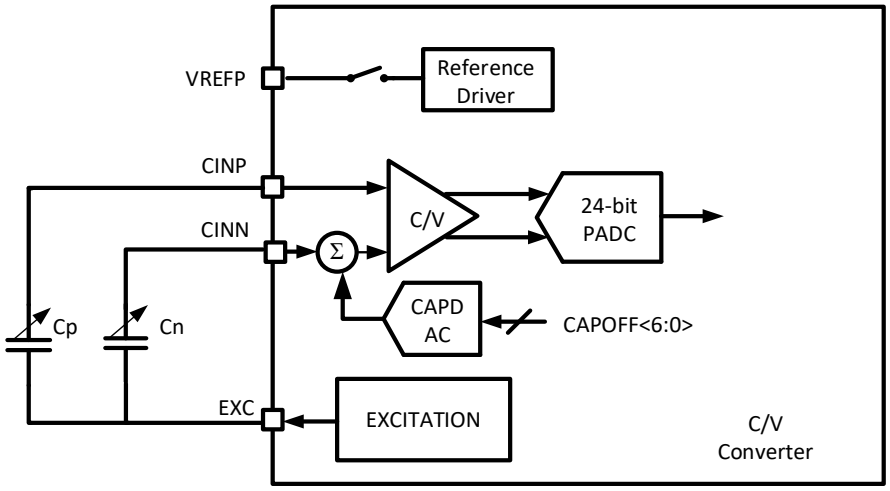


Figure 5. 2 C/V converter at Drive Mode (CV_MODE = 0)

When CV_MODE = 1, the NSC2860X is at Ground Mode, where the common plate of the external differential input capacitors is grounded as shown in Figure 5.3. Both CINP and CINN are driven by the square wave at EXC pin, so the differential input capacitance is converted to voltage through charge and discharge. The 24-bit ADC then converts the voltage to digital output. Since the NSC2860X measures the capacitance between CINP/CINN and ground, the parasitic capacitance at CINP/CINN would affect the measurement directly. Worse, the parasitic capacitance may be large and susceptible to environment interfere (such as displacement, humidity and so on). To exclude the parasitic capacitance, CINP and CINN can be shielded with EXC pin as shown in Figure 5.3. Ground Mode is more suitable especially when the common plate of the differential input capacitor cannot be driven by the chip directly.

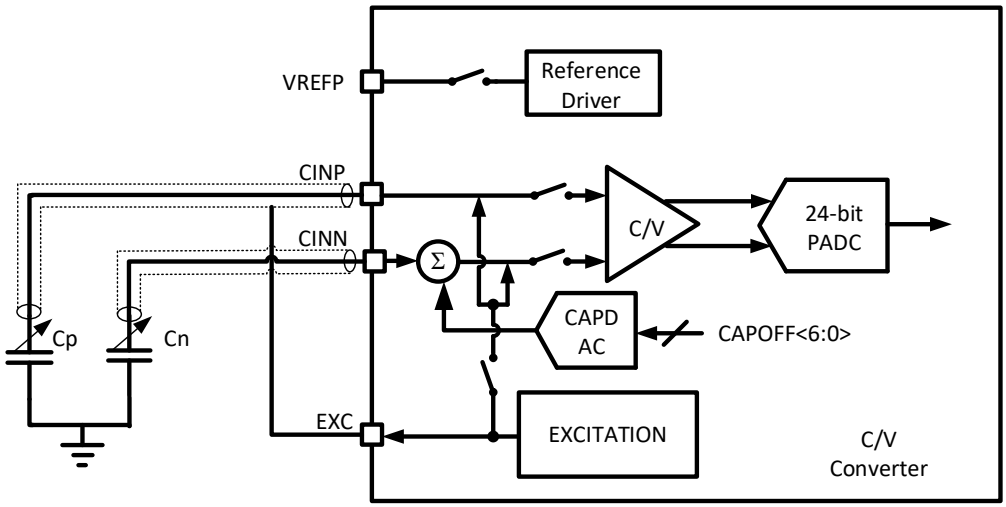


Figure 5.3 C/V converter at Drive Mode (CV_MODE = 1)

5.2.2. The measurement range of C/V converter

5.2.2.1. The differential input capacitance range

The PADC converts the analog output of C/V converter to digital output, which is filtered by digital filter with 24-bit digital output $PDATA_{RAW}$. $PDATA_{RAW}$ is expressed by the following expression.

$$PDATA_{RAW} = \frac{C_P - C_N - CAPOFF}{|C_{RANGE}|} * 2^{23}$$

CAPOFF is an internal offset compensated capacitance configured by CAPOFF<6:0>. The unit capacitance of CAPDAC is 0.5pF, so it's as large as 127*0.5pF = 63.5pF. CRANGE is the full scale range of C/V measurement configured by CV_RANGE<1:0> and CV_Gain as referred to Section 4.2. PDATARAW can be read from P channel data registers (Reg0x06, 07, 08) when RAW_P = 1. When RAW_P = 0, the built-in MCU will calibrate the sensor using sensor calibration coefficients and the data of temperature measurement. So the content of PDATA registers are the sensor output after temperature calibration.

5.2.2.2. The common mode input capacitance range

When the differential input capacitance is not out of range ($PDATA_{RAW}$ is in between ± 1), the common mode capacitance range is expressed by the following expression.

$$C_{CM} = \frac{C_P + C_N + CAPOFF}{2} < C_{CM\_RANGE}$$

C_{CM_RANGE} is also related to CV_RANGE<1:0> as referred to Section 4.2.

5.2.3. Digital Filter

The bandwidth and output data rate (ODR) of the digital filter can be set by 'ODR_P'. ODR can be set from 2.4 KHz to 2.5 Hz. The lower ODR, the lower noise the PADC output will have, in the cost of slower time response. Table 5.1 shows the effective number of bits (ENOB) of PADC output with different ODR_P settings. The relationship of ENOB with RMS noise is:

$$ENOB_{RMS} = 24 - \log_2(RMS_{ADC})$$

RMSADC is the RMS value of ADC output noise in LSB. The relationship between RMS ENOB (ENOBRMS) and noise free ENOB (ENOBNF) is shown as below:

$$ENOB_{NF} = ENOB_{rms} - 2.7$$

Table 5.1 ENOBRMS of PADC under different ODR settings

ODR_P(Hz)	C_{RANGE}=±16pF	C_{RANGE}=±12pF	C_{RANGE}=±8pF	C_{RANGE}=±4pF
2400	15.6	15.7	16.0	15.9
1200	15.9	15.9	16.2	16.0
600	16.3	16.2	16.7	16.6
300	16.7	16.6	17.1	17.0
150	17.1	17.2	17.6	17.4
75	17.6	17.6	18.0	17.8
37.5	18.1	18.1	18.5	18.4
18.75	18.6	18.6	19.1	18.7
10	19.0	19.1	19.4	19.3
5	19.6	19.5	19.9	19.8
2.5	20.1	20.0	20.4	20.1

*For ODR of 10Hz, two filter settings can be selected but with the same $ENOB_{RMS}$

*When ODR_P=10Hz, the 50 or 60Hz notch filter will be activated. User can choose the proper notch filter for different applications. The error of the clock rate is designed to be less than 1% to minimize the effect to notch filter ability.

5.3. Analog Module 2: Temperature Measurement Channel

The temperature measurement channel is to measure the working temperature of the sensor for the temperature compensation of the sensed signal. This channel works independently of the primary channel. The NSC2860X supports both internal temperature sensor and external temperature sensor, selected by register bit 'EXT_TEMP' bit. The temperature sensor's output is digitized by a 24-bit ADC (TADC) and also digital filtered. The ODR setting of the temperature measurement channel is the same as the primary signal channel, set by 'ODR_T'. When the temperature difference between the sensor element and the NSC2860X chip is acceptable, internal temperature sensor can be used. Otherwise, a proper external temperature measurement scheme should be chosen, such as diode, RTD, NTC or the bridge resistor itself, etc. Through different 'RAW_T' setting, either the direct TADC data or the calibrated temperature data can be read from 'TDATA' registers.

5.3.1. Internal Temperature Sensor

The internal temperature sensor is factory calibrated, with its calibration coefficients stored at EEPROM registersreg0xC1, reg0xC2 and reg0xC3. When 'RAW_T' is set to 0 and 'GAIN_T' is set to 4X, the NSC2860X can provide a temperature reading in degree Celsius, in the format of

$$T = TDATA / 2\text{^}16 + 25\ ℃$$

For example, 'TDATA=0x1FF24B' corresponding to 56.95°C. The relationship between the noise of the internal temperature sensor and 'ODR_T' setting is shown in Table 5.2.

Table 5.2 RMS Noise of Internal Temperature Sensor under different ODR_T

ODR (Hz)	2400	1200	600	300	150	75	37.5	18.75	10	5	2.5
RMS Noise in ℃	0.0079	0.0060	0.0045	0.0038	0.0032	0.0020	0.0015	0.0011	0.0008	0.0008	0.0007

5.3.2. External Temperature Sensor

When external temperature sensor mode is selected, the temperature sensing signal input from the TEMP pin is buffered for TADC conversion.

The reference voltage of the TADC is also VREF. The gain of the TADC can be 1X, 2X and 4X. The relationship between $TDATA_{RAW}$ and the temperature input is

$$TDATA_{RAW} = VTEMP * GAIN\_T / VREF * 2^{23}$$

When RAW_T = 0, the built-in MCU calibrated the offset, sensitivity and nonlinearity of the measured temperature signal. Please refer to calibration application note for the detailed description.

The output data rate of TADC can be set by 'ODR_T', similar as the primary signal channel. The relationship between ODR_T and the ENOB of TADC is shown in Table 5.3.

Table 5.3 ENOB of TADC under different ODR_T (External temperature sensor mode)

ODR_T (HZ)	ENOB		
	GAIN_T=1	GAIN_T=2	GAIN_T=4
2400	17.7	17.5	16.9
1200	18.1	17.9	17.2
600	18.5	18.1	17.2
300	18.8	18.3	17.4
150	19.1	18.5	17.6
75	19.5	18.9	18.0
37.5	19.4	18.6	17.6
18.75	19.9	18.7	18.1
10	20.2	19.4	18.5
5	20.2	19.6	18.5
2.5	20.9	19.9	18.8

5.4. Analog Output Stage

The analog output stage of the NSC2860X consists of a 16-bit DAC and an output buffer with feedback network. Through register configuration and external connection, the NSC2860X provides a lot of output modes such as absolute voltage output (0~5V, 0~3.3V, 0~1.2V), ratio-metric voltage output (0~AVDD), 0~10V voltage output, PDM output, PWM output, 4~20mA current loop. The output mode of analog output stage can be configured by 'OUT_MODE' registers, which is an independent configuration from analog front-end ADC.

5.4.1. 16-bit DAC

The voltage output of the DAC is expressed by the following equation.

$$VOUT = \frac{DAC\_DATA<15:0>}{2\text{^}16} * VFSDAC$$

'DAC_DATA' stores the DAC input data in unsigned format. VFSDAC is DAC full scale range, which is configured by 'DAC_REF'. When 'RAW_P' = 0, the 'DAC_DATA' is updated by the internal MCU with the calibrated output data. The DAC full scale range is clamped by the clamping voltage configured by 'CLAMP_HIGH' and 'CLAMP_LOW'.

The low clamping voltage is defined by the following equation.

$$VOUT\_LOW = \frac{CLAMP\_LOW<7:0>}{2\text{^}9} * VFSDAC$$

The high clamping voltage is defined by the following equation.

$$VOUT\_HIGH = (1 - \frac{CLAMP\_HIGH<7:0>}{2\text{^}9}) * VFSDAC$$

5.4.2. Voltage Output

When OUT_MODE=000b, analog output stage is configured as voltage output mode. A class-AB output buffer is used to drive large load and the OUT pin and FBN pin should be shorted together as shown in Figure 5.4. The OUT pin and FBN pin can be also shorted internally as to reduce the chip pin count by setting OUT_MODE=001b. The gain of output buffer is configured by 'DAC_REF' to provide several types of full scale output range, such as absolute output (0~5V, 0~3.3V, 0~1.2V) and ratio-metric output (0~AVDD), as listed in Table 5.4. The internal bandgap reference is used for absolute output.

Table 5.4 DAC_REF' and output mode

DAC_REF<1:0>	Output Mode	Output Voltage Range
2'b00	Absolute	0~5V
2'b01	Absolute	0~3.3V
2'b10	Absolute	0~1.2V
2'b11	Ratio-metric	0~AVDD

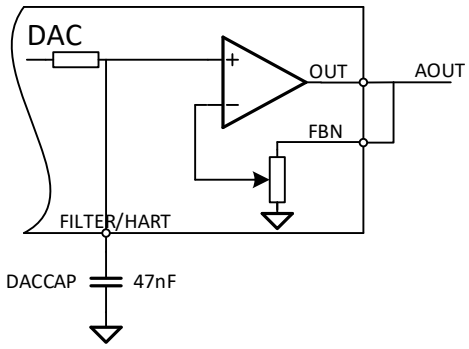


Figure 5.4 Configuration for voltage output mode(external feedback mode)

0~10V full scale output range is also available as shown in Figure 5.5 with a few external components, where DAC_REF<1:0>= 2'b00.

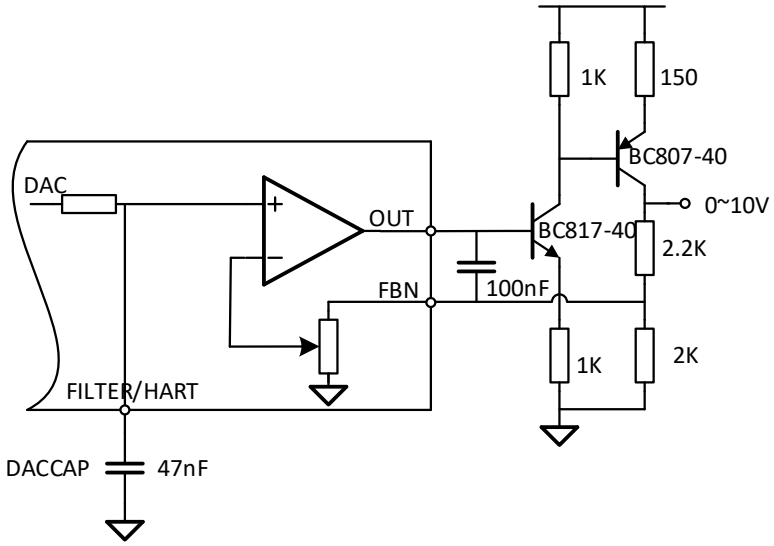


Figure 5.5 Configuration for 0~10V output mode

5.4.3. 4~20 mA Current Loop

When OUT_MODE=01xb and DAC_REF<1:0>=00b, analog output stage is configured as 4~20mA current loop mode. Internal bandgap reference with very low temperature drift is used for DAC reference. When using 50ohm external reference resistor, the loop current can be expressed as followed.

$$ILOOP = \frac{DAC\_DATA<15:0>}{2\text{^}16} * 24mA$$

The loop current transfer function is also shown in Figure 5.7. The minimum of ILOOP is about 1.5mA, which is determined by the self-operation current of the NSC2860X. To not exceed 4mA lower limit for 4~20mA current loop, the total current consumed by the NSC2860X and sensor element should be less than 3.5mA.

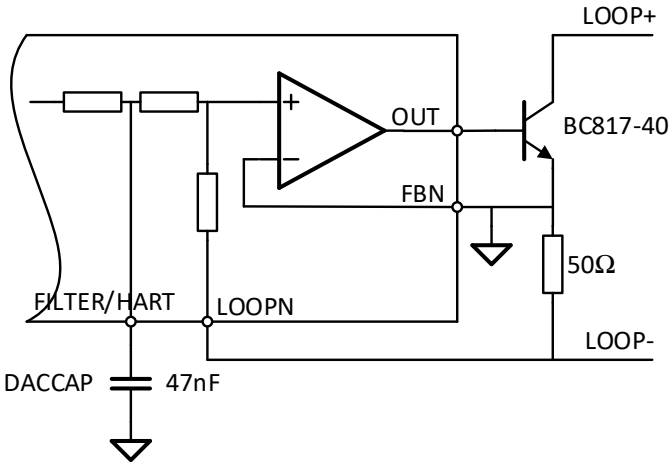


Figure 5.6 Configuration for 4~20mA current loop mode

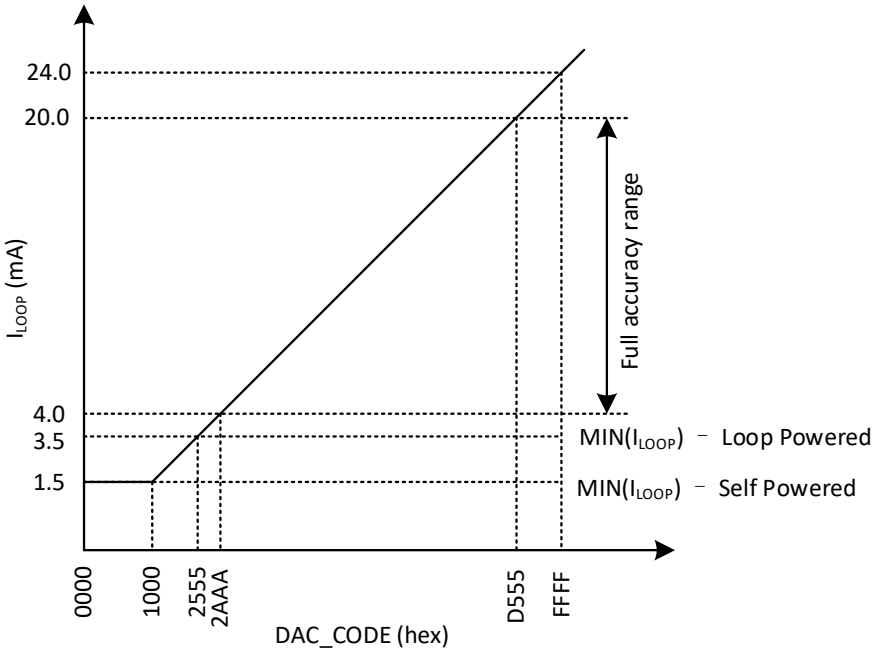


Figure 5.7 Loop current transfer function

The FILTER/HART pin can not only be used for noise filtering, but also for HART communication in current loop mode. As shown in Figure 5.8, the 500mVpp HART signal can be modulated into current loop as 1mApp current through a 470pF capacitor.

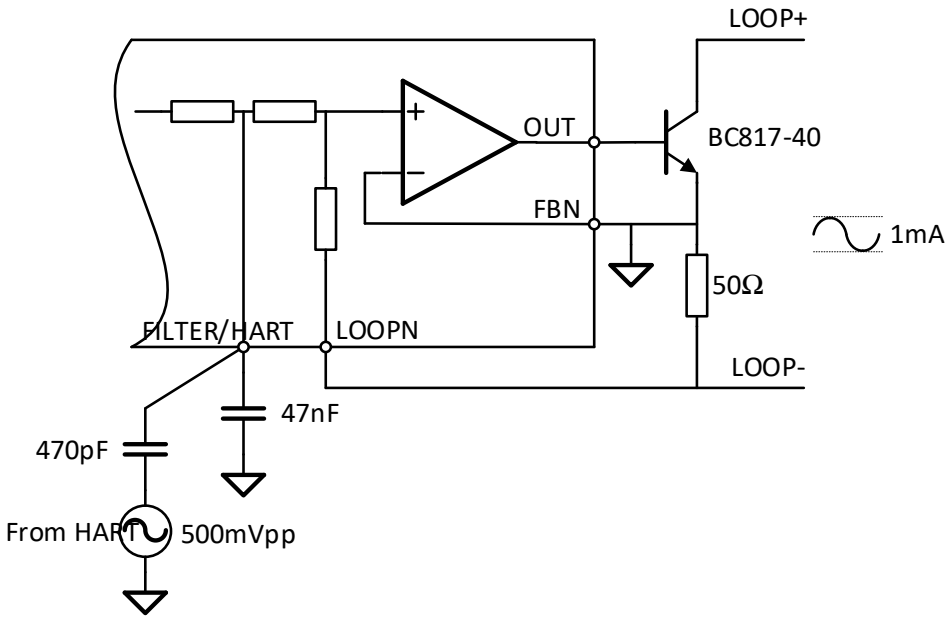


Figure 5.8 Configuration for HART communication

5.4.4. PDM

When 'OUT_MODE' = 100b, analog output stage is configured as PDM output mode, The 'DAC_DATA' is converted to 1 bit PDM single by a 1-order modulator internally and outputted through OUT pin. An external RC filter should be connected to OUT pin to filter the PDM signal to analog voltage. Digital isolation output can also be realized by external level shifter and isolation device. 'PDM_FREQ' is used to set the PDM output frequency. The equivalent output resistance at OUT pin is about 20ohm. As a result, when using external RC filter, the equivalent resistance load should be less than 20Kohm as to make sure the output error is less

than 1‰. Two-stage low pass RC filter in series is recommended as shown Figure 5.9. Some RC filter examples are provided in Table 5.5.

Table 5.5 RC filter examples for PDM output

R1 (kOhm)	*C1 (nF)*	*R2 (kOhm)*	*C2 (nF)*	*Ripple（mV/V）*	*0~90% Settling Time(us)*
100	22	100	22	0.12	14
100	100	0	0	2.5	24
100	220	0	0	1.2	50

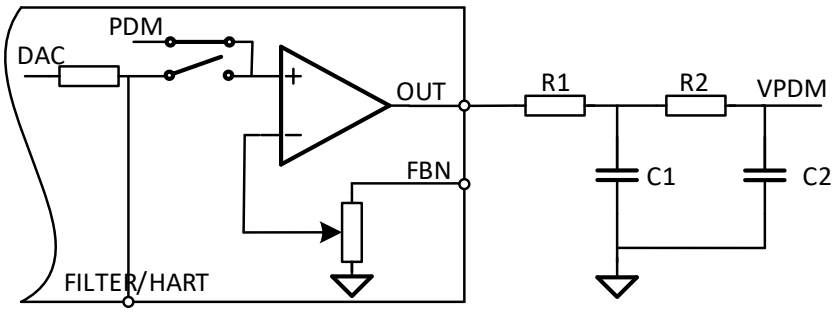


Figure 5.9 RC filter for PDM output

5.4.5. PWM

Both primary signal channel and temperature measurement channel support PWM output.

When 'OUT_MODE'=101b, primary channel output data will present on the OUT pin in the PWM format. The PWM carrier frequency is fixed at 300Hz, and the PWM output duty cycle is decided by DAC_DATA<15:4> with 12-bit resolution.

$$Duty\_Cycle = \frac{DAC\_DATA<15:4>}{4096}$$

When 'TOUT_EN'= 1 and the chip is not in OWI mode, the OWI pin is used as the output pin for Temperature Channel data in PWM format and the PWM output duty cycle is defined as follow:

$$Duty\_Cycle = \frac{TDATA<23:12>}{4096}$$

5.5. Power Management and Sensor Driver

The NSC2860X internally includes a precision bandgap reference with very low temperature drift, less than 0.1% during full temperature range (-40~85°C). This reference voltage is used in the constant voltage or current driving circuits for sensors, JFET regulator, clock generator and ADC/DAC etc.

5.5.1. JFET Regulator

By tuning the gate of external JFET (for example, BSS169) through VGATE pin, the JFET regulator integrated in the NSC2860X can convert the external high voltage supply to 5V (JFET_LVL=0) or 3.3V (JFET_LVL=1) and supply it to the VDDHV pin (Figure 5.10). The voltage of VSUP can be up to 36V.

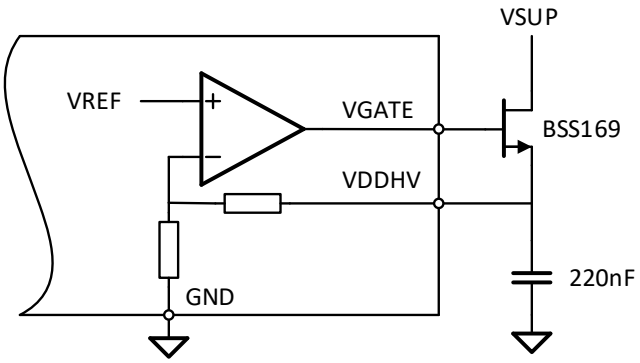


Figure 5.10 Regulation with external JFET

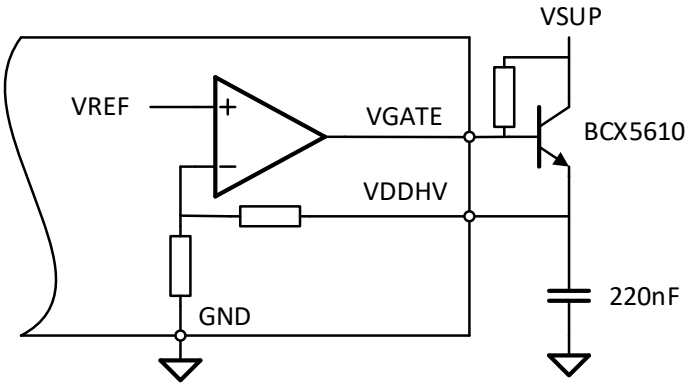


Figure 5.11 Regulation with external NPN Bipolar

5.5.2. Internal LDO

A 1.8V LDO is integrated in the NSC2860X to provide power supply for the internal digital circuits. A 100nF decoupling capacitor should be connected at DVDD pin externally.

5.5.3. Power on Reset

A POR block is integrated in the NSC2860X for power on reset and EEPROM loading. When AVDD<2.5V, the chip is in reset state. After AVDD > 2.5V, the POR output is released and EEPROM is loaded afterwards. The POR circuits have 100mV hysteresis, that is, the chip won't go into the reset state again until the AVDD is dropped as low as 2.4V.

5.6. Built-in MCU Core and Control Logics

5.6.1. Function Mode

The NSC2860X has five different working modes: single mode, continuous mode, command mode and programming mode. User can choose alternate mode by writing different values in COMMAND register CMD<7:0>.

5.6.1.1. Single mode (CMD<7:0> = 0x01/0x02)

Writing 0x01 or 0x02 to register CMD<7:0> will make the NSC2860X enter single mode from command mode. In this mode, the chip will enter command mode after data conversion being completed once. CMD<7:0> will return to 0x00 simultaneously. The conversion time of single mode depends on ODR_P and ODR_T settings.

5.6.1.2. Continuous mode (CMD<7:0> = 0x03)

Writing 0x03 to CMD<7:0> will make NSC2860X enter continuous mode. In this mode, the primary signal ADC channel and temperature ADC channel will refresh the PDATA and TDATA registers at a stated ODR continuously. Writing 0x00 to CMD<7:0> can make NSC2860X exit continuous mode.

If RAW_P or RAW_T is set to 1, the ADC conversion results will be put into the 'PDATA' or 'TDATA' directly. Otherwise, the embedded MCU will use the latest temperature data to calibrate primary ADC channel output data every time its measurement completed. .

When the register bit 'INT_EN' = 1, the SDO_DRDYB pin is used to indicate that a new data is ready for reading via the serial interface with an active low voltage level, and this pin will come back to high level after the data reading or about 100us before next new data's coming.

Even without the SDO_DRDYB pin, the shadow registers inside the NSC2860X can also guarantee a non-glitch reading by keeping the 'PDATA' and 'TDATA' registers stable during once serial interface reading. Note that, the multiple bytes of one measured data should be read out together in once multi-byte serial interface reading command.

5.6.1.3. Command mode (CMD<7:0> = 0x00)

In this mode, access to all configuration registers is allowable and the chip keeps in a relative low power state.

5.6.1.4. Programming mode (CMD<7:0> = 0x33)

Only in this mode, EEPROM can be programmed. Please refer to chapter 5.5 for detailed information about EEPROM operation.

5.6.2. EEPROM

64 bytes EEPROM is contained in the NSC2860X to store the chip configurations and sensor calibration coefficients.

5.6.2.1. Loading

The contents of the EEPROM will be loaded into the EEPROM registers automatically after power up or soft reset with the CRC checking. If the calculated CRC result does not match with what stored in the EEPROM, the 'CRC_ERROR' bit will be set. Another status register bit 'LOADING_END' will be set after the loading completes.

5.6.2.2. Programming

Writing EEPROM registers will not program the EEPROM directly. The contents of the EEPROM registers will be programmed into the EEPROM by following sequence:

1. Set the register byte 'COMMAND' (Reg0x30) with 0x33, to enter EEPROM programming mode.
2. Writing the register byte 'EE_PROG' (Reg0x6A) with 0x1E or 0x9E, to start EEROM programming.

When 0x1E is used, the built-in MCU will first compare the register contents with the EEPROM contents, and only erase and program the bytes with the difference. If 0x9E is used, all EEPROM contents will be erased and then programmed. The programming time is different in these two modes. It is recommended to use 0x7E for programming.

During EEPROM programming, a new CRC check code will be generated according to the contents of the EEPROM registers and will be programmed to the EEPROM simultaneously. The content of the 'EE_PROG' register will automatically come back to 0x00 to indicate the programming is done. A re-powering up or soft reset is needed to reload the EEPROM contents back to the EEPROM registers to check the programmed value.

5.6.2.3. Lock and Unlock

The EEPROM inside the NSC2860X can be locked by setting the 'EEPROM_LOCK' bit then programming it into the EEPROM. After locked, the EEPROM cannot be programmed again, and only a special EVA-kits provided by NOVOSENSE can unlock it.

5.6.3. Built-in MCU Core

The NSC2860X is integrated with a built-in MCU core, which performs the signal processing, sensor calibration, EEPROM loading and programming etc. The MCU's program code is pre-stored in the internal ROM, which cannot be modified by customers. Please contact NOVOSENSE if a customized MCU program code is needed.

5.6.4. Calibration

The calibration flow inside the NSC2860X is divided into two steps. The first is the ADC calibration, which can erase the offset and sensitivity error induced by the ADC. The other is sensor calibration, which can compensate the sensor with offset, sensitivity, up to the 2nd order offset temperature drift, up to the 2nd order sensitivity temperature drift, up to the 3rd order non-linearity, and the totally calibration error is less than 0.1% of the full span. Please refer to application note details.

5.7. Serial Interface

Three different serial interfaces (OWI, SPI and I2C) are supported in the NSC2860X to configure registers, program EEPROM and pulling measured data. When register bit 'OWI_WINDOW' = 0, the time between 2.5ms and 20ms after powering up is defined as the OWI entering window. If a special 24 bits OWI entering pattern is detected via OWI pin in this window, the chip enters OWI communication mode, otherwise enters I2C or SPI communication mode. Then, CSB pin is used to further select between I2C and SPI methods, high voltage level or floating indicates the I2C method, low voltage level indicates the SPI method. When 'OWI_WINDOW' = 1, the OWI window becomes infinite length.

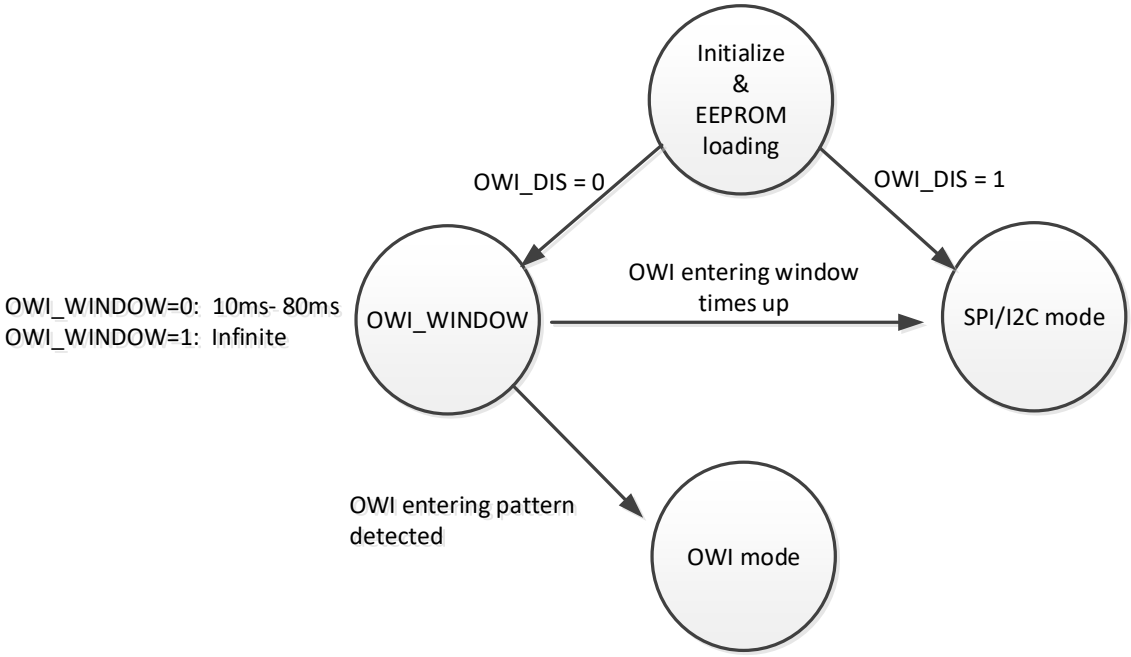


Figure 5.12 Definition of serial communication mode

5.7.1. OWI Interface

The NOVOSENSE self-owed One Wire Interface (OWI) protocol is integrated in the NSC2860X. This protocol identifies the data bit transferred by the duty cycle of one rising-to-rising period. Duty cycle more than 5/8 means a logical 1, and less than 3/8 means a logical 0.

5.7.1.1 Timing Specification

Table5.6 OWI Timing Specification

Symbol	*Description*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*
t_{period}	OWI bit period		20		700	us
t_{pulse_0}	Duty cycle for 0		1/8	1/4	3/8	t_{period}
t_{pulse_1}	Duty cycle for 1		5/8	3/4	7/8	t_{period}
t_{start}	Start low pulse time		20		4000	us
t_{stop}	Stop condition time		2			t_{period}

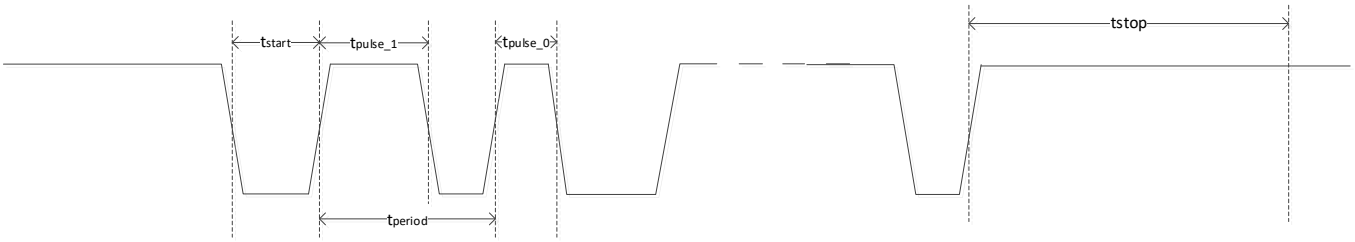


Figure 5.13 OWI Timing

5.7.1.2 Enter OWI Mode

If 'OWI_WINDOW' = 0, the time between 2.5ms and 20ms after powering up is OWI entering window. If a special 24 bits OWI entering pattern (0xB5A6C9, as shown below) is detected via OWI pin in this window, the chip enters OWI communication mode.

If 'OWI_WINDOW' = 1, the OWI window's length becomes infinite.

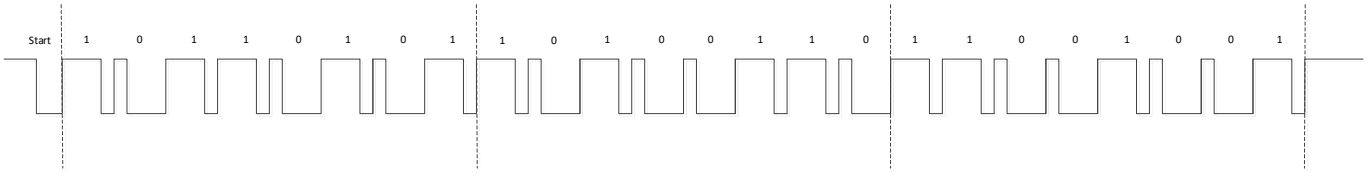


Figure 5.14 OWI Entering Pattern

In OWI communication, the bit period is determined by the period of the last bit of OWI entering pattern, and cannot be changed during the entire communication, so the bit period during OWI communication should keep the same as the OWI entering pattern.

5.7.1.3 OWI Protocol

The OWI protocol used is defined as follows:

a) Idle State

During inactivity of the bus, OWI line is pulled-up to high voltage level.

b) Start Condition

When OWI line is in idle state a low pulse (return to high) with a pulse width between 20us to 4ms indicates a start condition. Every command must be initiated by a start condition sent by the master. The master can only generate the start condition when the OWI line is in idle state.

c) Stop Condition

After the write or read operation ends, the bus comes back to the idle state automatically. During any time of a transmission, the bus can be set back to the idle state by forcing the OWI line constant high or low voltage level for at least two times of the bit period (tperiod)

d) Addressing

After the start condition, the master sends the addressing information, consisting of an 8-bit register address (MSB first), 2-bit byte number (NO. bits) and a read/write–bit (0–write, 1–read). The register address indicates which register you will write into or read from; the byte number indicates how many bytes will write/read continuously: 00: 1 byte, 01: 2 bytes, 10: 3 bytes, 11: 4 bytes; the read/write-bit indicates it a read operation (0) or write operation (1).

e) Write Operation

During transmission from master to slave (WRITE), the read/write bit is followed by 1/2/3/4 bytes (according to the byte NO. bits) transmitted data (MSB first), and the addressed register and follows will be refreshed to the written data after a stop condition.

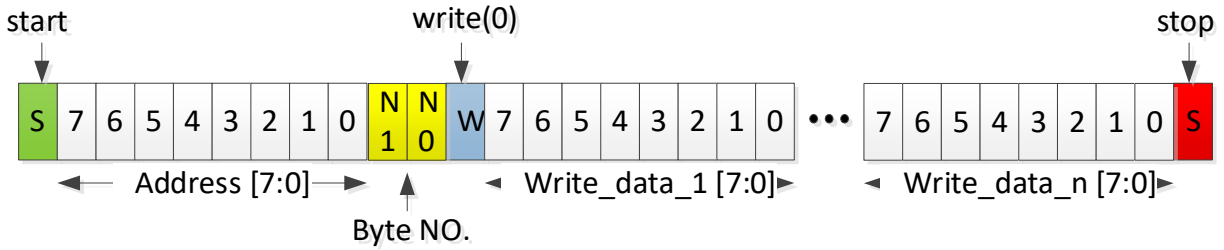


Figure 5.15 OWI Write Operation

f) Read Operation

During transmission from slave to master (READ), the master should set its OWI port as input after the read/write bit is sent, then the slave begins to transmit 1/2/3/4 bytes (according to the byte NO. bits) data (MSB first), which is contented in the addressed register and follows. Each data bytes include 8 bits of data and 2 bits of parity check code C1 and C0.

C1 = Read_data[7] ^ Read_data[5] ^ Read_data[3] ^ Read_data[1].

C0 = Read_data[6] ^ Read_data[4] ^ Read_data[2] ^ Read_data[0].

The master can check the transmission with the parity check code. After all data bytes transmitted, the slave goes back to idle state automatically.

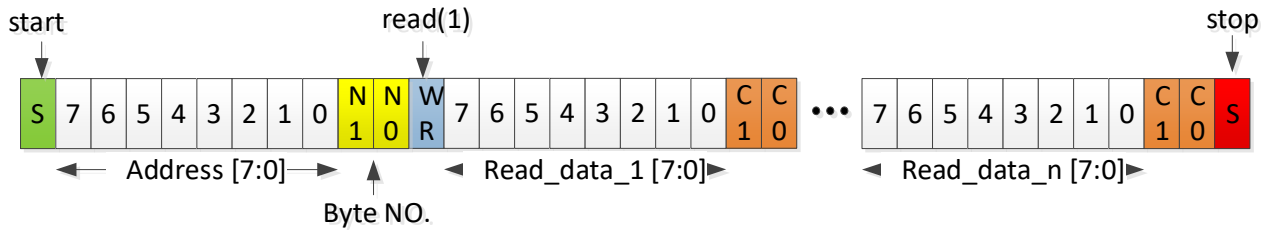


Figure 5.16 OWI Read Operation

5.7.1.4 Pins and Configurations

Two pins (OWI and OUT) and two register bits (OWI_AC_EN and OWI_WINDOW) are related to the OWI communication. Different applications can be supported via different configurations. Please refer to Table5.7 for details.

OWI_AC_EN: 0, single-port communication method with the OWI pin used for both input and output port, which is typically used in 0-5V analog output products. 1, dual-port communication method with the OWI pin as the slave input port and the OUT pin as the slave output port; this method is typically used in the 0-10V and 4-20mA products

OWI_WINDOW: 0, OWI mode should be entered between a 10ms and 80ms window after powering up. 1, the window is infinite, and the OWI mode can be entered any time after powering up.

Table5.7 Pin configurations for OWI communications

OWI_AC_EN	*OWI_WINDOW*	*Windows*	*Input Port*	*Output Port*	*Output Mode*	*OUT pin state mode*	*Shorten OUT and OWI*	*Typical Applications*
0	0	10ms-80ms	OWI	OWI	OD	HiZ	Supported	3-wire modules with 0～5V output (Short OUT and OWI pins)，external pull-up resistor is needed
0	1	Infinite	OWI	OWI	OD	Signal Output	Not Supported	Cases that signal out and OWI communication are used simultaneously, external pull-up resistor is needed.
1	0	10ms-80ms	OWI	OUT	Push-Pull	OWI output	Supported	3-wire modules with 0-10V output, 2-wire modules with 4-20mA output. 0-5V output modules with big load capacitor
1	1	Infinite	OWI	OUT	Push-Pull	OWI output	Supported	Isolated Transmitter using OWI/OUT pins for Isolated communication

5.7.1.5 Dual-Port OWI Communication (OWI_AC_EN=1)

As described in 5.7.1.4, a special dual-port OWI communication is supported by the NSC2860X for applications in 4-20mA and 0-10V output products with no extra communication wires added. The protocol is shown in Figure 5.17, with the OWI pin as the slave input port, and the OUT pin as the slave output port.

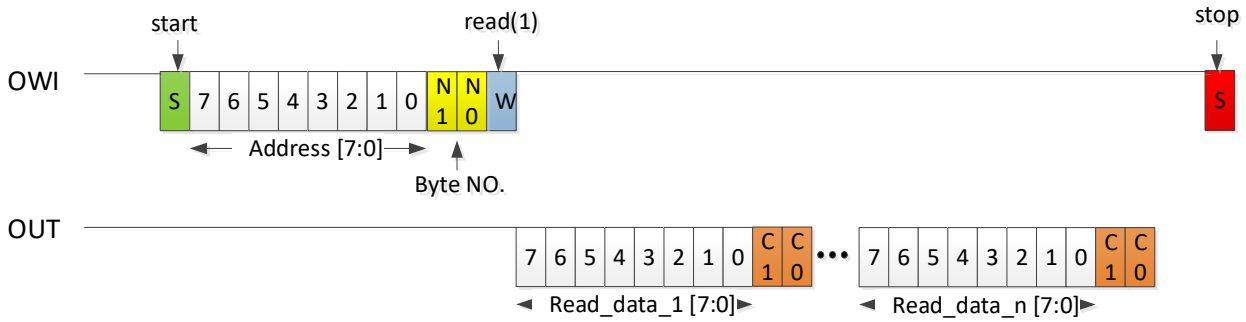


Figure 5.17 Dual Ports OWI Communication

As shown in figure 5.18, in 4-20mA applications, data transmission from the master to the chip is implemented by adding a square-waved signal on the power supply wire and AC coupling it onto the OWI pin with an external capacitor. The chip to master transmission data is modulated to the loop current (1: 10mA, 0: 4mA) and can be read out by the master through a comparator circuit. Limited by the response time of the current loop, the bit period of this OWI communication method should be no less than 100us. The advantage of this kind of communication method is that the LOOP+/LOOP- wires are multiplexed for communications and no extra communication wires needed. Similarly, in the 0-10V applications, data transmission from the master to chip is also implemented by signal coupling from the power supply to the OWI pin and data from chip to the master is put on the OUT pin. Also, only three wires (VDD, GND, OUT) are needed for a 0-10V product with no extra communication wires.

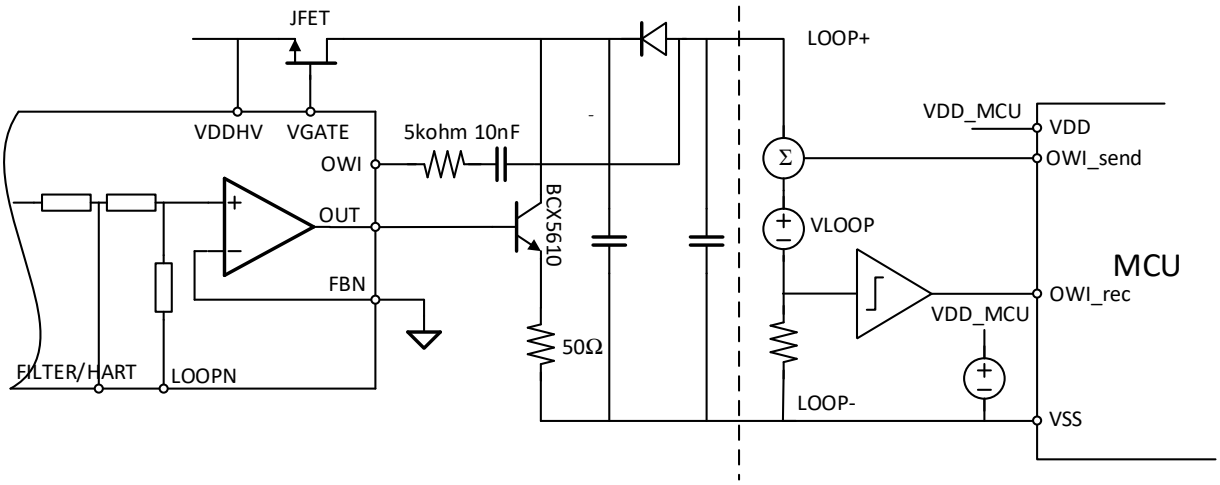


Figure 5.18 Typical circuit for the dual ports OWI communication in the 4~20mA applications

5.7.1.6 Quit OWI Mode

Writing Reg0x61 with 0x5d during OWI mode can temporarily or permanently quit the OWI communication for output voltage or current measuring. The register byte 'OWI_QUIT_CNT' is used to set the quit time with the LSB = 50ms (0x00 means permanently quit), and the chip will be back into OWI mode again after the quit time's up.

5.7.2. SPI Interface

Table5.8 SPI interface specifications

Symbol	*Parameter*	*Condition*	*Min*	*Max*	*Unit*

f_{sclkB}	Clock frequency	Max load on SDIO or SDO = 25pF		10	MHz
t_{sclk_l}	SLCK low pulse		20		ns
t_{sclk_h}	SLCK high pulse		20		ns
T_{sdi_setup}	SDI setup time		20		ns
T_{sdi_hold}	SDI hold time		20		ns
T_{sdo_od}	SDO/SDI output delay	Load = 25pF		30	ns
		Load = 250pF		40	ns
T_{csb_setup}	CSB setup time		20		ns
T_{csb_hold}	CSB hold time		40		ns

The figure below shows the definition of the SPI timing given in Table 5.8.

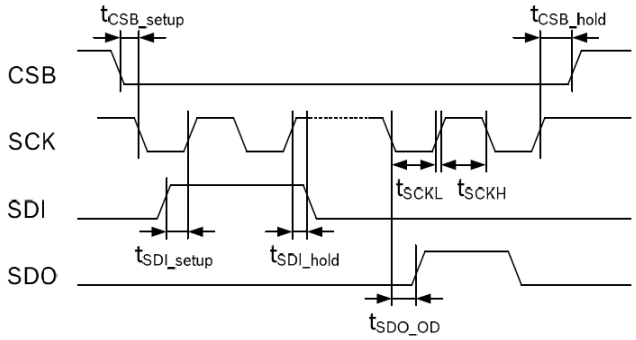


Figure 5.19 SPI timing diagram

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in Figure 5.20, the instruction phase is divided into several bit fields.

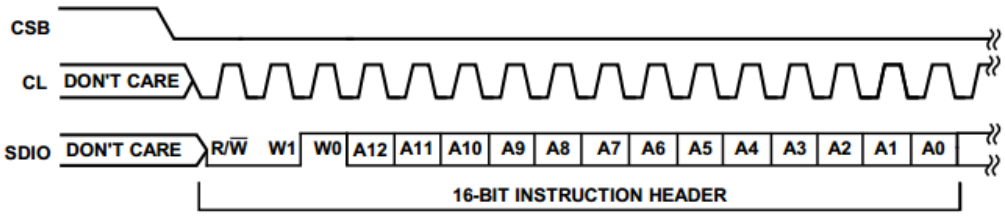


Figure 5.20 Instruction Phase Bit Field

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read is being requested, otherwise indicates it is a write operation.

W1 and W0 represent the number of data bytes to transfer for either read or write (Table 5.9). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a non-byte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions high. CSB is not allowed to stall during the streaming process.

The remaining 13 bits represent the starting address of the data sent. If more than one word is being sent, sequential addressing is used, starting with the one specified, and it either increments (LSB first) or decrements (MSB first) based on the mode setting.

Table5.9 W1 and W0 settings

W1:W0	Action	CSB stalling
00	1 byte of data can be transferred.	Optional
01	2 bytes of data can be transferred.	Optional
10	3 bytes of data can be transferred.	Optional
11	4 or more bytes of data can be transferred. CSB must be held low for entire sequence; otherwise, the cycle is terminated.	No

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). This can be one or more bytes of data. All data is composed of 8-bit words.

Data can be sent in either MSB-first mode or LSB-first mode (by setting 'LSB_FIRST' bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed.

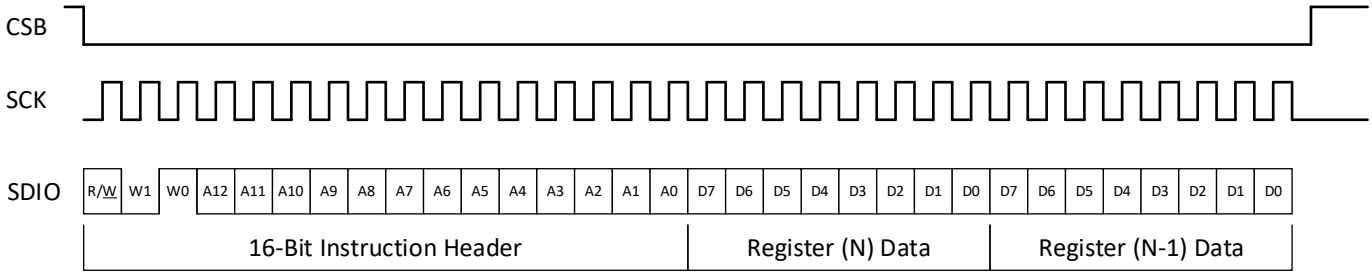


Figure 5.21 MSB First Instruction and Data Phases

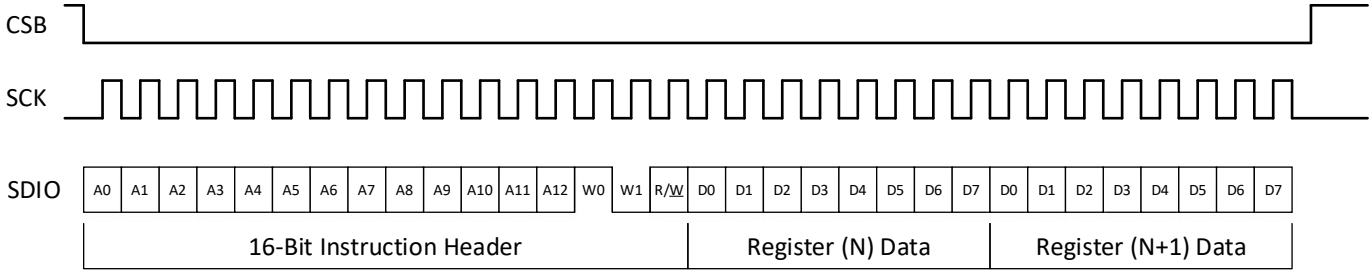


Figure 5.22 LSB First Instruction and Data Phases

Register bit 'SDO_ACTIVE' is responsible for activating SDO on devices. If this bit is cleared, then SDO is inactive and read data is routed to the SDIO pin. If this bit is set, read data is placed on the SDO pin. The default for this bit is 1, making SDO active.

5.7.3. I2C Interface

I2C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I2C device address of NSC2860X is shown below. The LSB bit of the 7bits device address is configured via SDO/ADDR pin.

Table5.10 I2C Address.

A7	A6	A5	A4	A3	A2	A1	W/R
1	1	0	1	1	0	1	0/1

Table5.11 Electrical specification of the I2C interface pins

Symbol	Parameter	Condition	Min	Max	Unit

f_{scl}	Clock frequency			400	kHz
t_{LOW}	SCL low pulse		1.3		us
t_{HIGH}	SCL high pulse		0.6		us
t_{SUDAT}	SDA setup time		0.1		us
t_{HDDAT}	SDA hold time		0.0		us
t_{SUSTA}	Setup Time for a repeated start condition		0.6		us
t_{HDSTA}	Hold time for a start condition		0.6		us
t_{SUSTO}	Setup Time for a stop condition		0.6		us
t_{BUF}	Time before a new transmission can start		1.3		us

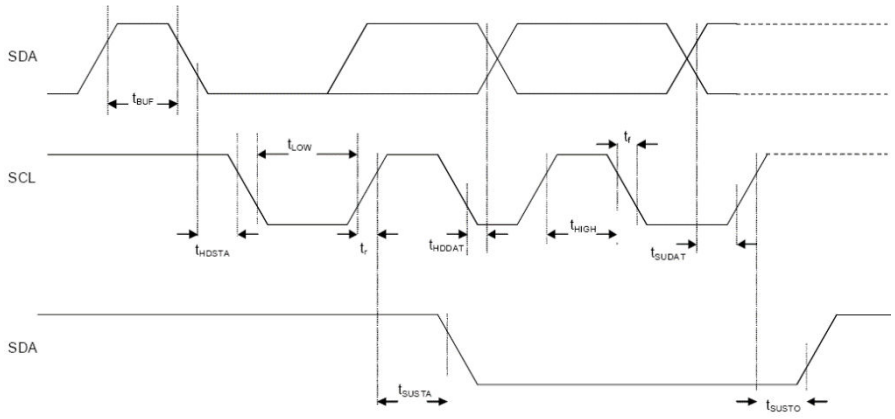


Figure 5.23 I2C Timing Diagram

The I2C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change value at SDA only when SCL is low.

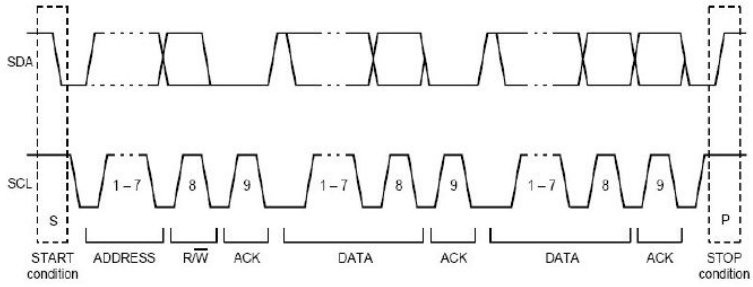


Figure 5.24 I2C Protocol

NSC2860X can support single byte and multiple bytes operation. The data format is shown in the figure below.

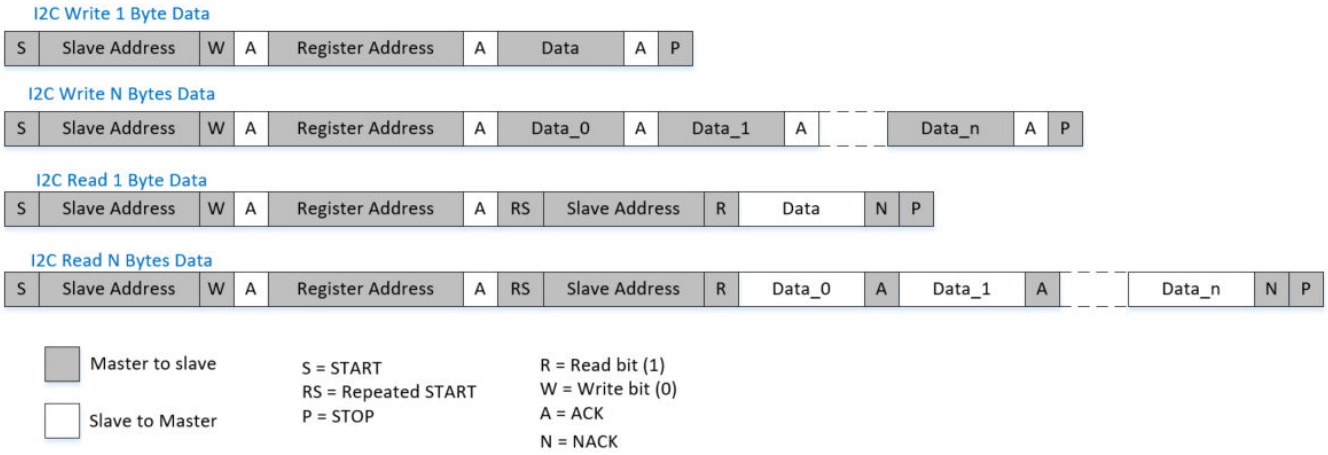
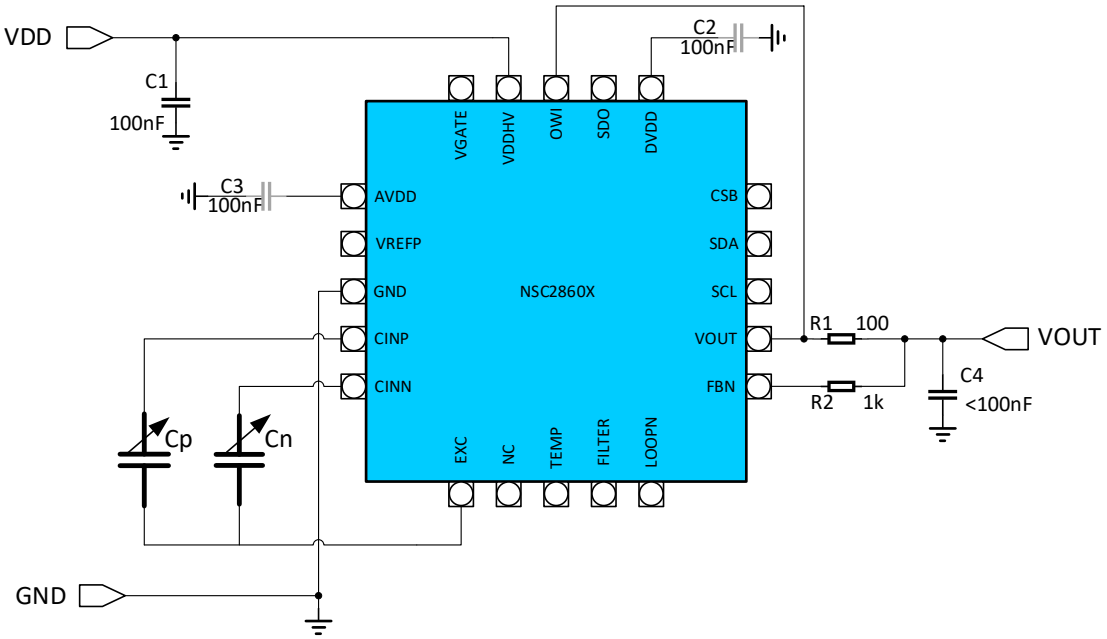


Figure 5.25 I2C Transfer Format

6. Application Note

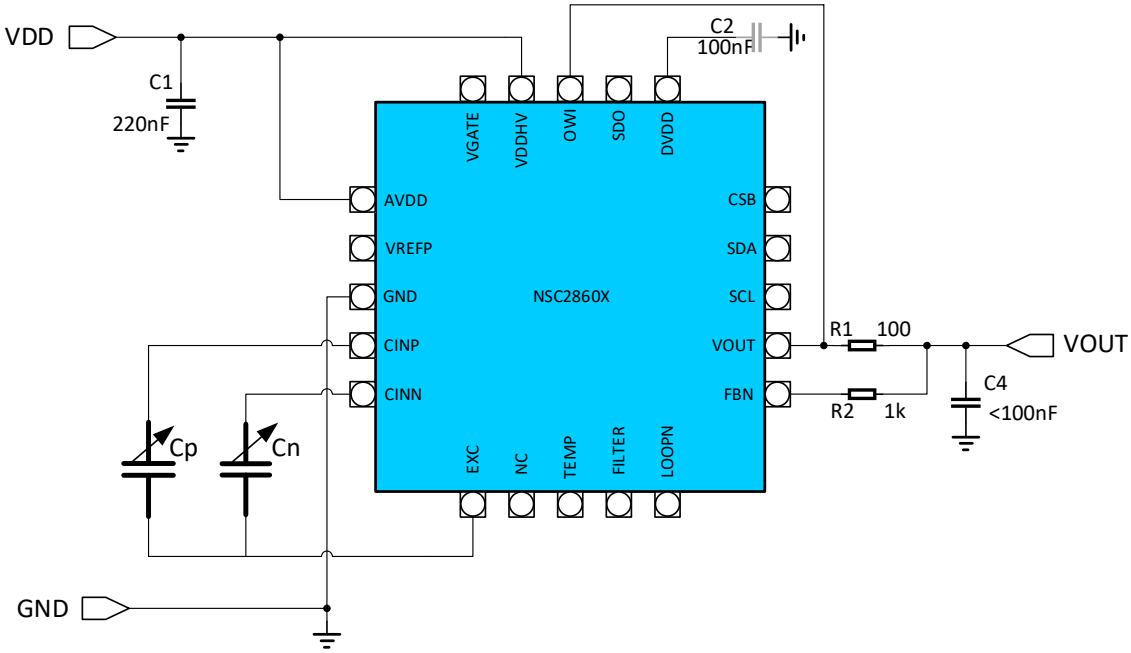
6.1. Typical Application 1: 0~5V Voltage Output with VDDHV Supply

This application uses VDDHV power supply and is able to provide overvoltage protection. However, the accuracy of the ratio-metric voltage output is slightly worse because of the VDDHV to AVDD circuit.

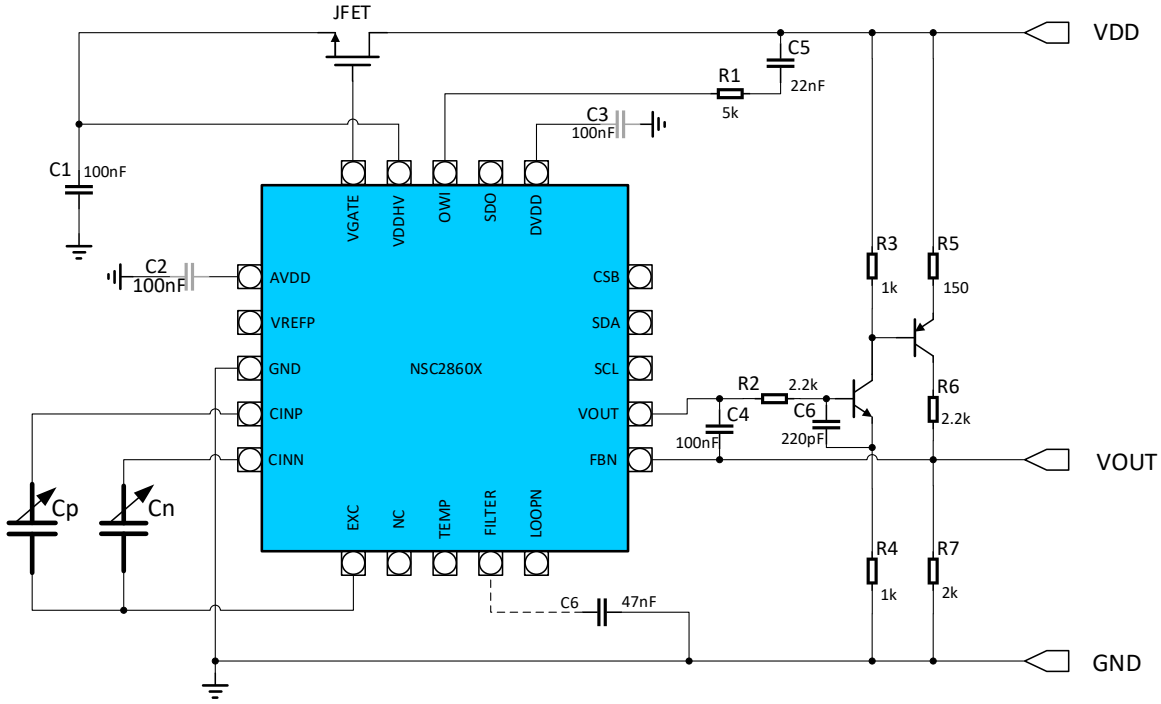


6.2. Typical Application 2: 0~5V Voltage Output with AVDD Supply

If you want to improve the accuracy of ratio-metric voltage output mode, then you need to be powered by AVDD. And it is recommended to connect AVDD and VDDHV together.

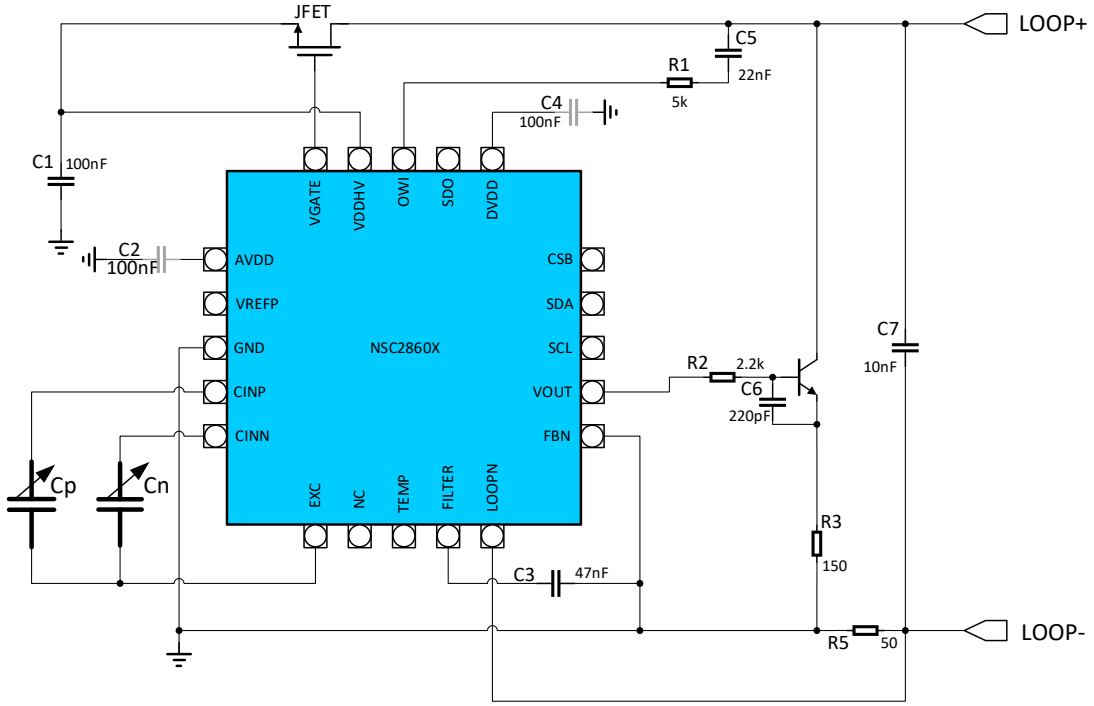


6.3. Typical Application 3: 0~10V Voltage Output



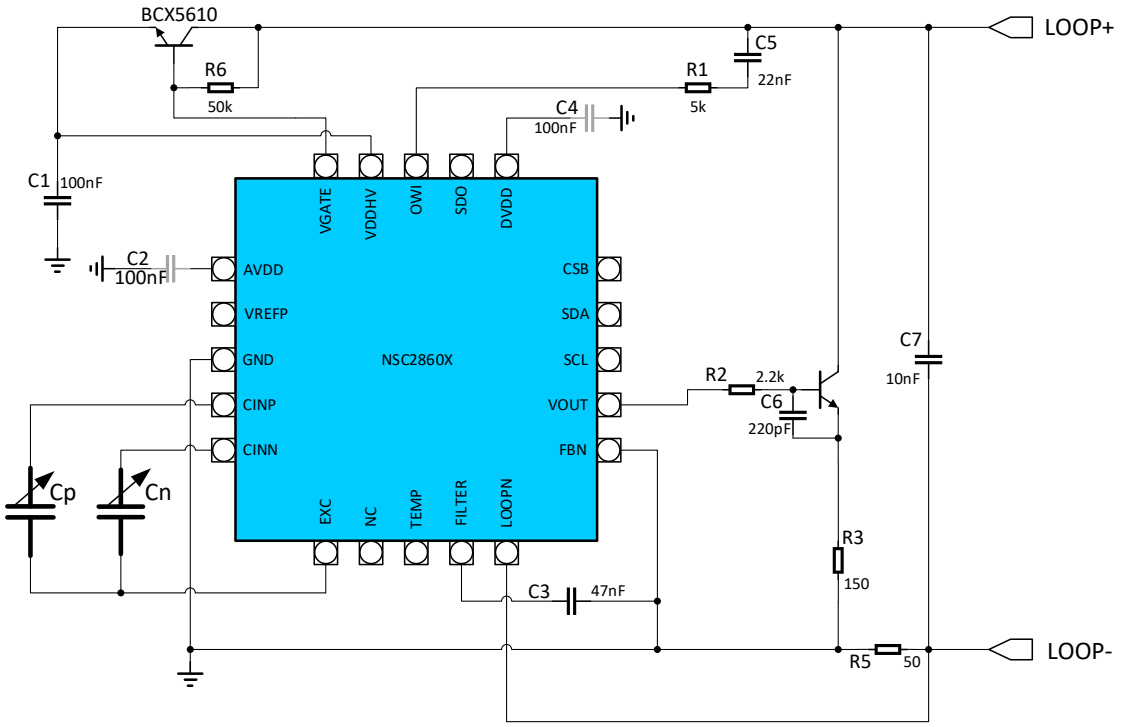
6.4. Typical Application 4: 4~20mA Output with JFET

The NSC2860X is power by an external JFET supply. R5 is a 50ohm low-temperature drift precision resistor used for voltage feedback. It only needs two lines to achieve power supply, current transmitter and OWI communication.

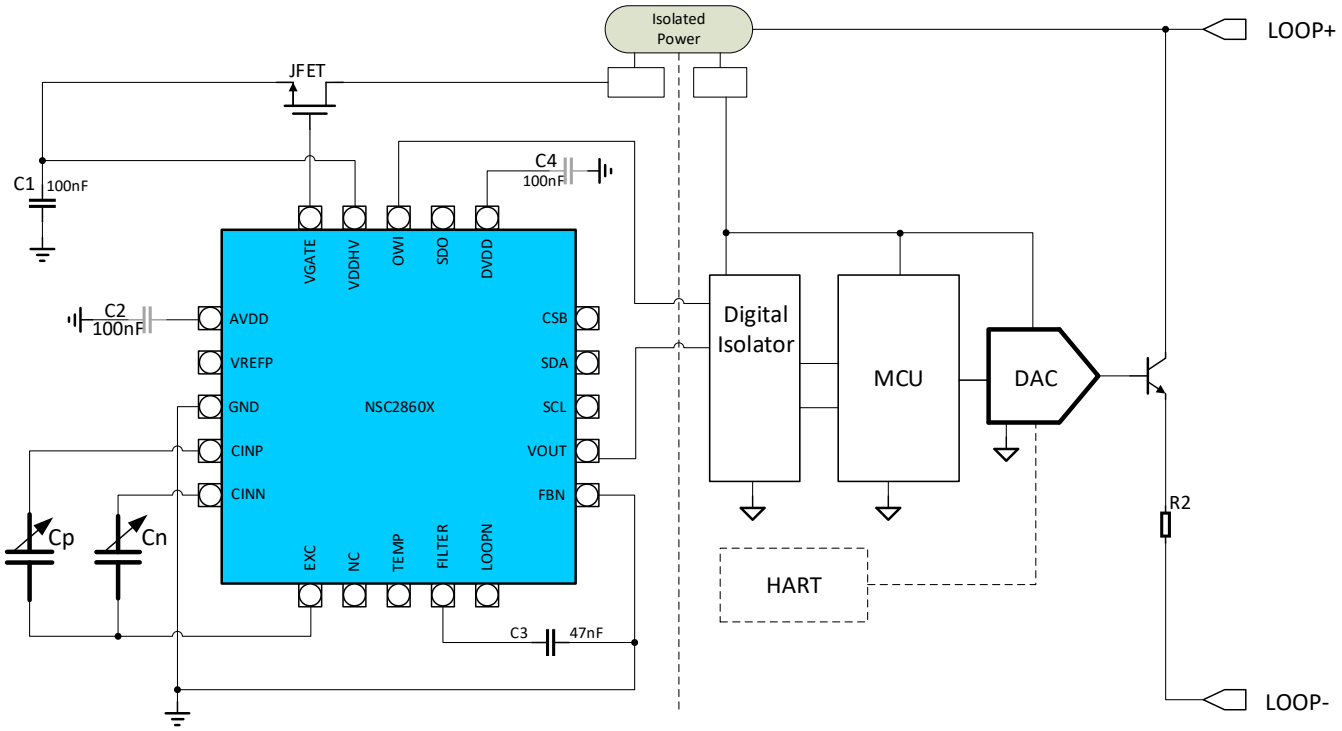


6.5. Typical Application 5: 4~20mA Output with BJT

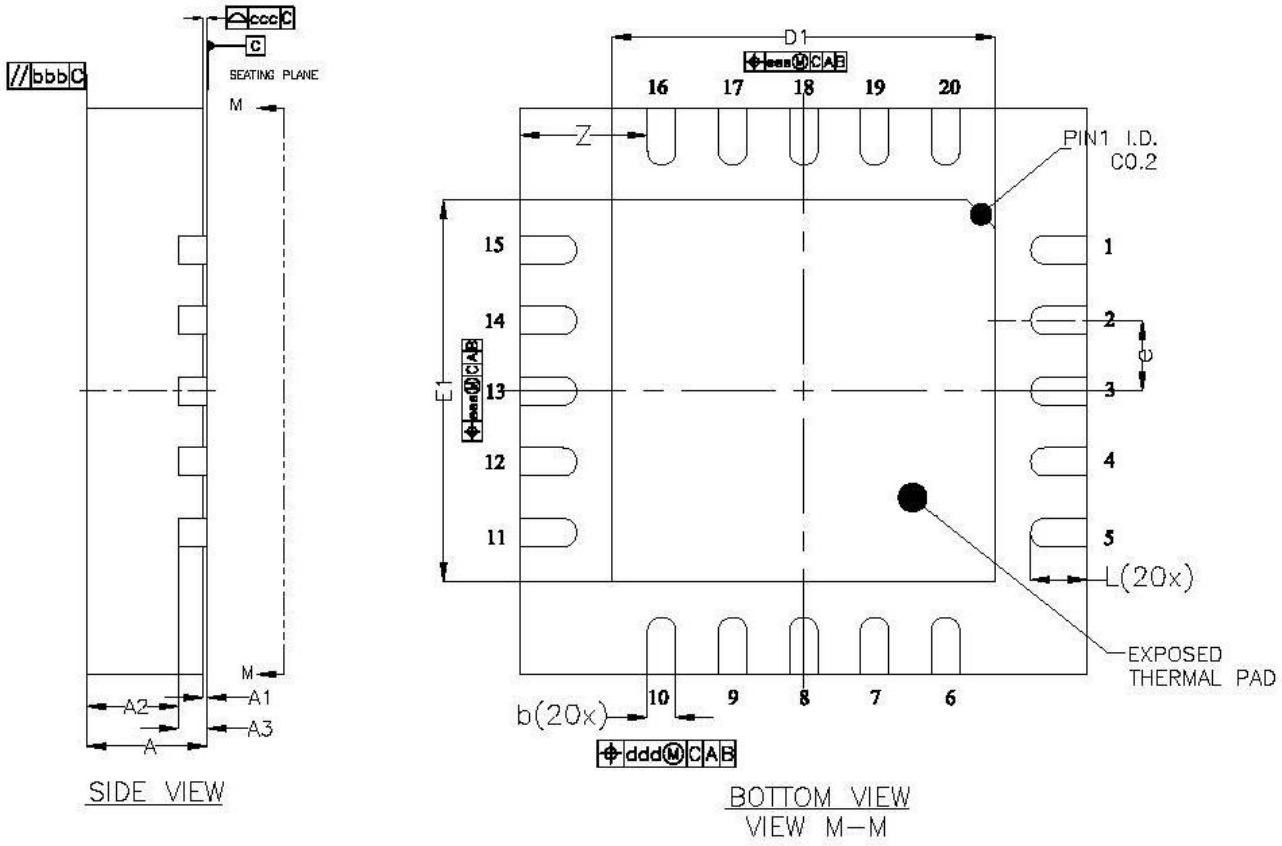
Compared to application 6.4, an NPN BJT with a 50kΩ resistor is used instead of the FET.



6.6. Typical Application 6: Isolated 4~20mA Output

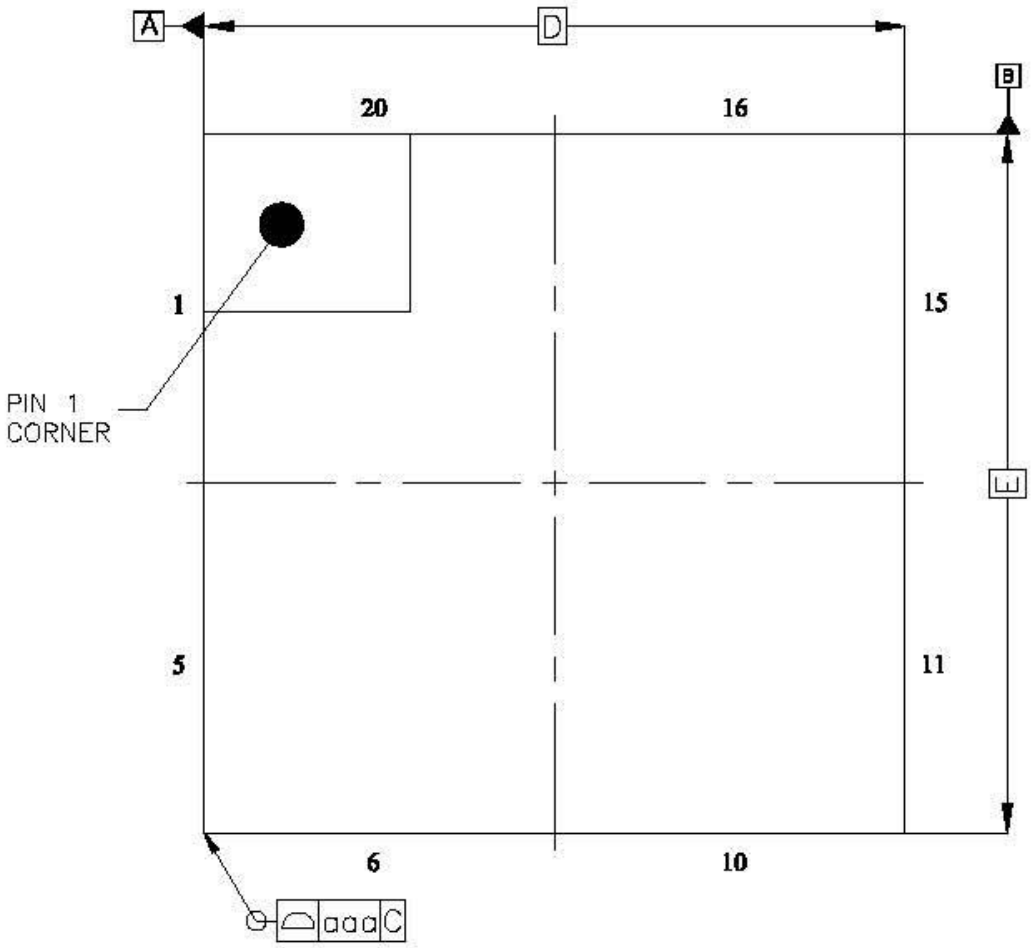


7. Package Information



NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.



TOP VIEW

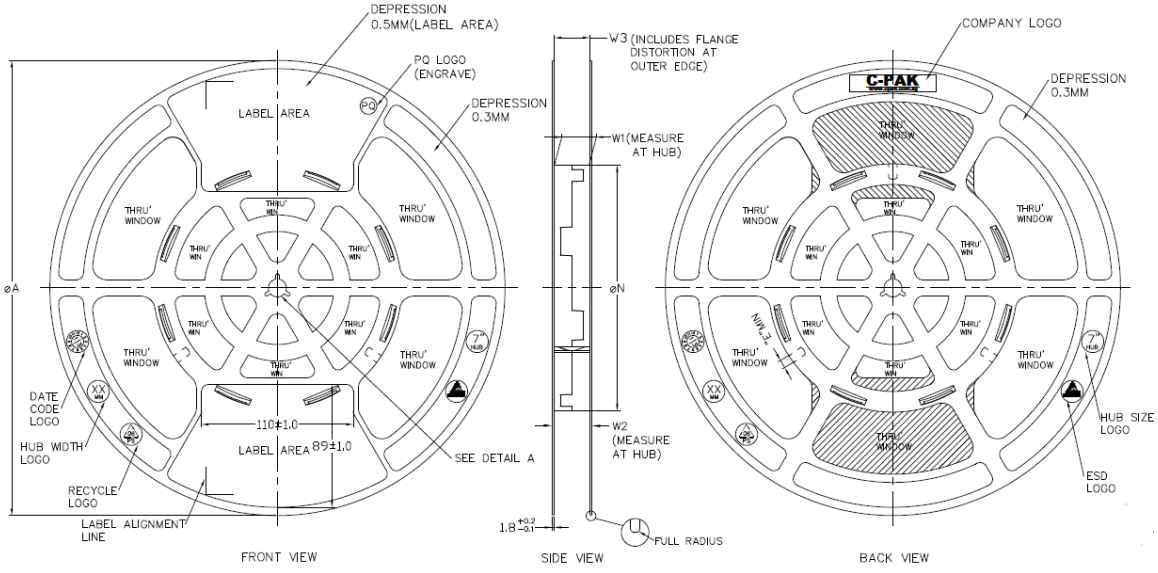
DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0.00	—	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D	3.95	4.00	4.05
	Y	E	3.95	4.00	4.05
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D1	2.65	2.70	2.75
	Y	E1	2.65	2.70	2.75
LEAD LENGTH		L	0.35	0.40	0.45
LEAD EDGE TO PKG EDGE		Z	0.9 REF		
Tolerance of form and position					
PACKAGE EDGE TOLERANCE	aaa		0.1		
MOLD FLATNESS	bbb		0.1		
COPLANARITY	ccc		0.08		
LEAD OFFSET	ddd		0.1		
EXPOSED PAD OFFSET	eee		0.1		

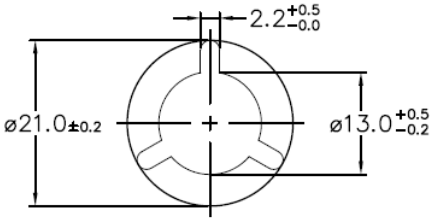
Figure 7.1 QFN20 Package Shape and Dimension in millimeters

8. Ordering Information

Part Number	Temperature	MSL	Package Type	SPQ
NSC2860X-DQNR	-40 to 125℃	3	QFN20	2500

9. Tape and Reel Information





ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{8} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

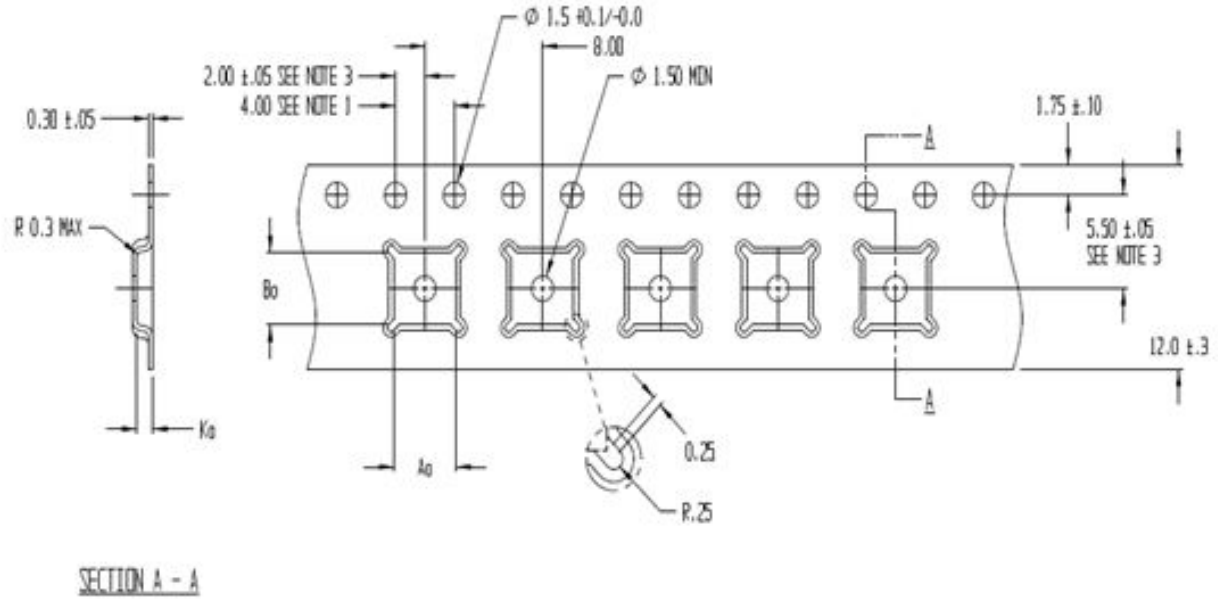
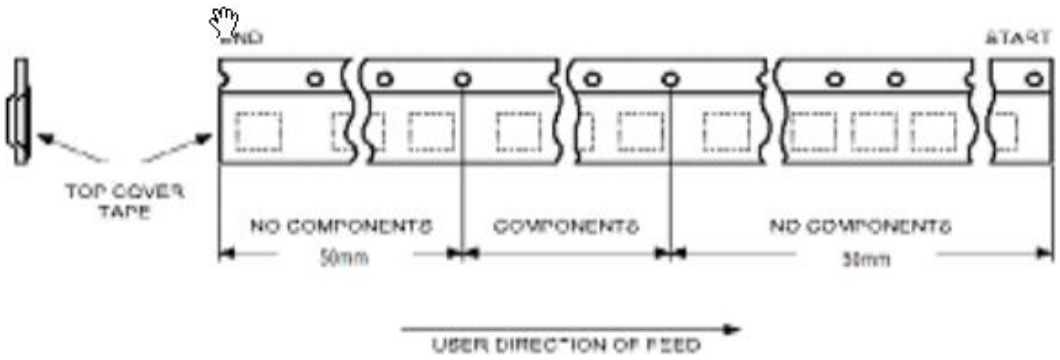
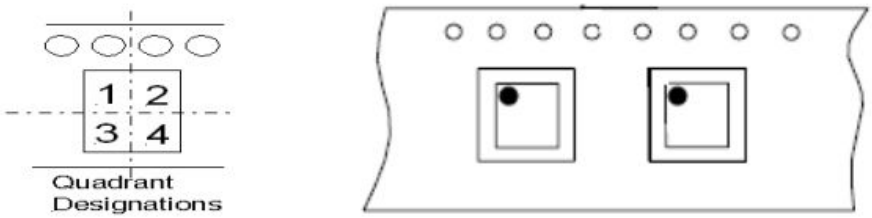


Figure 12.1 Tape and Reel Information of QFN20

Package	A0 (mm)	B0 (mm)	K0 (mm)	F (mm)	P1 (mm)	W (mm)
QFN20	4.25	4.25	1.1	5.50±0.05	8.00±0.1	16.0±0.3



Pin 1 is located at the first quadrant, as shown in the following figure.



10. Revision History

Revision	Description	Date
1.0	Initial Version.	2022/5/15

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