NSi6801

Single-Channel Isolated Gate Driver

Datasheet (EN) 1.0

Product Overview

The NSi6801 is a single-channel isolated gate driver which is pin-compatible for popular opto-coupled gate driver. It can source and sink 5A peak current. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 32V. While the input circuit imitates the characters of LEDs, it has performance advantages compared to standard opto isolated gate drivers, including better reliability and aging performance, higher working temperature, shorter propagation delay and smaller pulse width distortion.

As a result, the NSi6801 is suitable to replace opto-isolated driver in high reliability, power density and efficiency switching power system.

Key Features

- Isolated single-channel driver
- Pin compatible, drop in upgrade for opto isolated gate drivers
- Driver side supply voltage: up to 32V with UVLO
- 5A peak source and sink output current
- High CMTI: ±150kV/us
- 75ns typical propagation delay
- 30ns maximum pulse width distortion
- Operation ambient temperature: -40°C ~125°C
- RoHS-compliant packages:
  - SOIC-6 wide body (SOW6)
  - DUB-8

Safety Regulatory Approvals

- UL recognition: 5700V_{RMS} SOW6 and 5000V_{RMS} DUB8 for 1 minute per UL1577
- DIN VDE V 0884-11:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

Applications

- DC-to-AC solar inverters
- Motor drives
- UPS and battery chargers
- Isolated DC/DC and AC/DC power supplies

Device Information

Part Number	*Package*	*Body Size*
NSi6801x-DSWFR	SOW6	7.5mm × 4.68mm
NSi6801x-DDBR	DUB8	9.32mm × 6.4mm

Functional Block Diagram

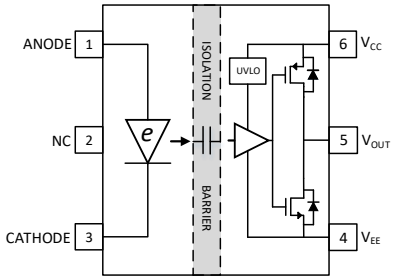

Figure 1. NSi6801 SOW6 Block Diagram

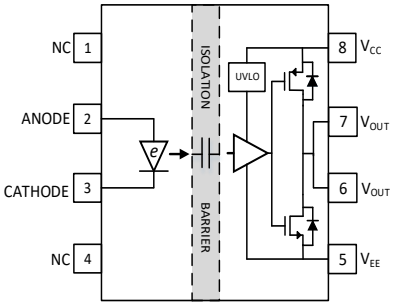

Figure 2. NSi6801T DUB8 Block Diagram

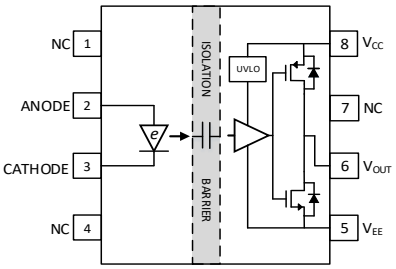

Figure 3. NSi6801L DUB8 Block Diagram

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1. Pin Configuration and Functions

NSi6801 SOW6 Top View

NSi6801T DUB8 Top View

NSi6801L DUB8 Top View

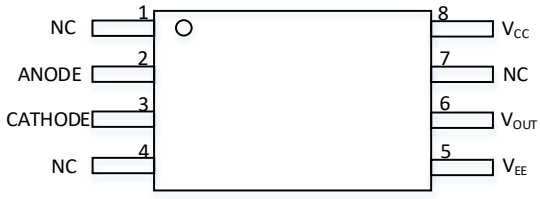


Table 1.1 NSi6801 Pin Configuration and Description

SYMBOL	*PIN NO.*			*FUNCTION*
	NSi6801 SOW6	*NSi6801T DUB8*	*NSi6801L DUB8*	
ANODE	1	2	2	Anode of LED emulator
CATHODE	3	3	3	Cathode of LED emulator
V_{EE}	4	5	5	Negative output supply rail
V_{OUT}	5	6, 7	6	Gate-drive output
V_{CC}	6	8	8	Positive output supply rail
NC	2	1, 4	1, 4, 7	No Connection

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Average Input Current	I_{F_AVG}		25	mA
Peak Transient Input Current	I_{F_PEAK}		0.2	A
Reverse Input Voltage	V_{R_MAX}		6.5	V
Driver Side Supply Voltage	V_{CC}-V_{EE}	-0.3	35	V
Output Signal Voltage	V_{OUT}	V_{EE}-0.3	V_{CC}+0.3	V
Operating Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C
Electrostatic discharge	V_{ESD_HBM}		±2000	V
	V_{ESD_CDM}		±1000	V

3. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(off)}$	-5.5	0.9	V
Driver Side Supply Voltage (NSi6801C)	V_{CC}-V_{EE}	14	32	V
Driver Side Supply Voltage (NSi6801B)	V_{CC}-V_{EE}	10	32	V
Ambient Temperature	T_A	-40	125	°C

4. Thermal Information

Parameters	*Symbol*	*NSi6801*		*Unit*
		SOW6	*DUB8*	
Junction–to-ambient thermal resistance	$R_{\theta JA}$	125	110	°C/W
Junction–to-top characterization parameter	Ψ_{JT}	30	30	°C/W

5. Specifications

5.1. DC Electrical Characteristics

(Unless otherwise noted, Typical values are at V_{CC} =15V, V_{EE}=GND, T_A=25°C. All min and max specifications are at T_J=-40°C to 150°C, V_{CC}=15V to 30V, V_{EE}=GND, $I_{F(ON)}$=7 mA to 16 mA, $V_{F(off)}$= –5.5V to 0.8V)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Driver Side Supply						
High Level Supply Current	I_{CCH}		1.7	3	mA	I_F=10mA, I_{OUT}=0mA
Low Level Supply Current	I_{CCL}		1.6	3	mA	V_F=0V, I_{OUT}=0mA
Driver Side Supply UVLO Threshold (NSi6801C, 13V UVLO Level)						
VCC UVLO Rising Threshold	V_{CC_ON}	12.6	13.2	13.7	V	I_F=10mA
VCC UVLO Falling Threshold	V_{CC_OFF}	11.7	12.3	12.7	V	
VCC UVLO Hysteresis	V_{CC_HYS}		0.9		V	
Driver Side Supply UVLO Threshold (NSi6801B, 9V UVLO Level)						
VCC2 UVLO Rising Threshold	V_{CC2_ON}	8.7	9.2	9.7	V	I_F=10mA
VCC2 UVLO Falling Threshold	V_{CC2_OFF}	8	8.5	9	V	
VCC2 UVLO Hysteresis	V_{CC2_HYS}		0.7		V	
Input Pin Characteristic						
Input Forward Threshold Current Low to High	I_{FLH}	1.5	2.7	4	mA	V_{OUT}>5V, Cg=1nF
Threshold Input Voltage High to Low	V_{FHL}	0.9			V	V_{OUT}<5V, Cg=1nF
Input Forward Voltage	V_F	1.8	2.1	2.4	V	I_F=10mA
Temp Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T$		0.34		mV/°C	I_F=10mA
Input Reverse Breakdown Voltage	V_R	6.5			V	I_R=10uA
Input Capacitance	C_{IN}		17		pF	f=1MHz
Output Pin Characteristic						
High Level Output Voltage	V_{OH}	V_{CC}-0.3	V_{CC}-0.15		V	I_{OUT}=-50mA, I_F=10mA
			V_{CC}			I_{OUT}=0mA, I_F=10mA
Low Level Output Voltage	V_{OL}		30	65	mV	I_{OUT}=50mA, V_F=0V
High Level Peak Output Current	I_{OH}		5.2		A	V_{CC}=15V, pulse width<10us
Low Level Peak Output Current	I_{OL}		5.4		A	V_{CC}=15V, pulse width<10us

5.2. Switching Electrical Characteristics

(Unless otherwise noted, Typical values are at V_{CC} =15V, V_{EE}=GND, T_A=25°C. All min and max specifications are at T_J=-40°C to 150°C, V_{CC}=15V to 30V, V_{EE}=GND, $I_{F(ON)}$=7 mA to 16 mA, $V_{F(off)}$= –5.5V to 0.8V)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Propagation Delay	t_{pLH}	50	75	100	ns	C_{LOAD}=1nF, f=20kHz (50% Duty Cycle)
Propagation Delay	t_{pHL}	50	69	100	ns	
Pulse Width Distortion $\lvert t_{PLH}-t_{PHL}\rvert$	t_{PWD}		6	30	ns	
Propagation Delay Difference Between Any Two Parts (t_{pHL}-t_{pLH}) (1)	PDD	-35		35	ns	
Output Rise Time (20% to 80%)	t_R		6	20	ns	
Output Fall Time (80% to 20%)	t_F		6	20	ns	
Common Mode Transient Immunity	CMTI	150			kV/us	

(1) The difference between t_{PHL} and t_{PLH} between any two parts under the same test condition, ensured by characterization.

5.3. Typical Performance characteristics

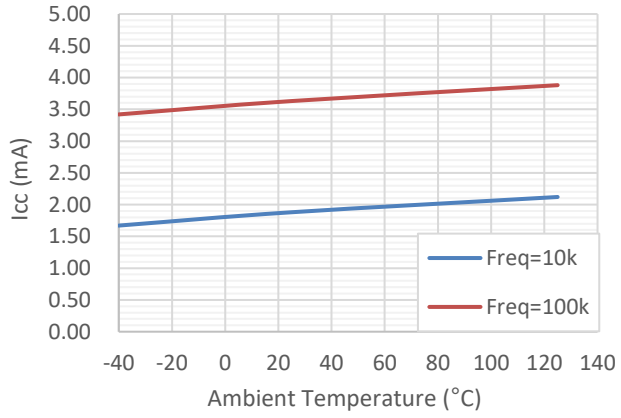


Figure 5.1 Supply currents versus Temperature

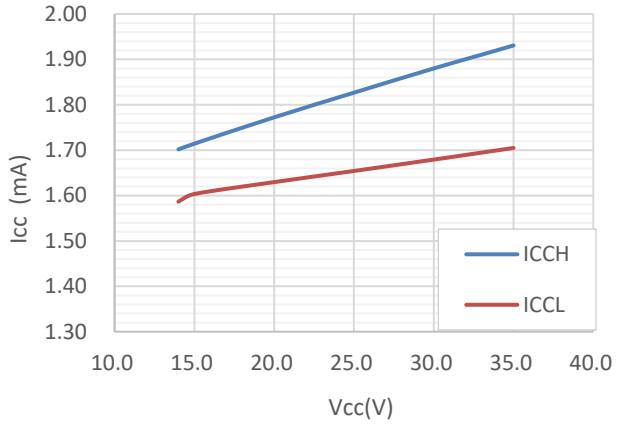


Figure 5.2 Supply current versus Supply Voltage

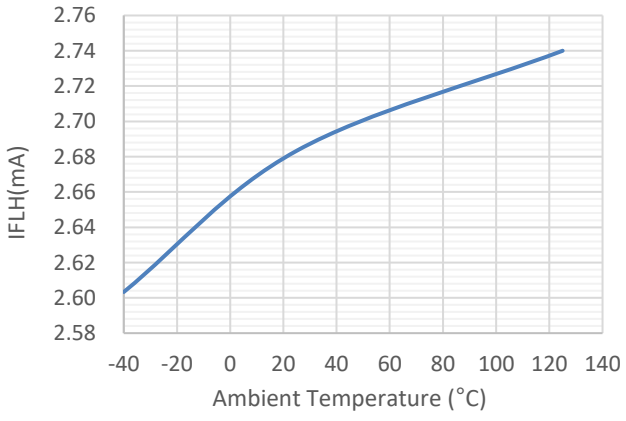


Figure 5.3 Forward threshold current versus Temperature

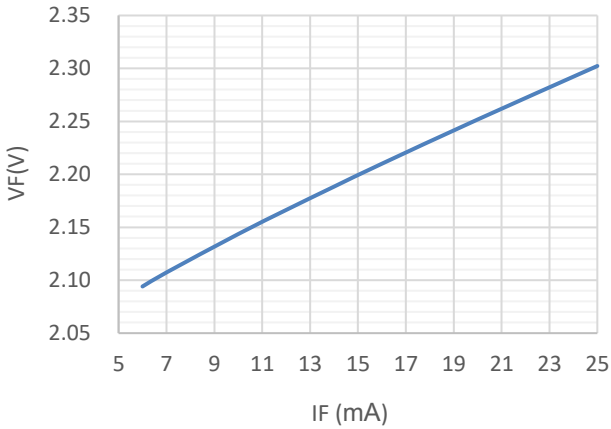


Figure 5.4 Forward current versus Forward voltage drop

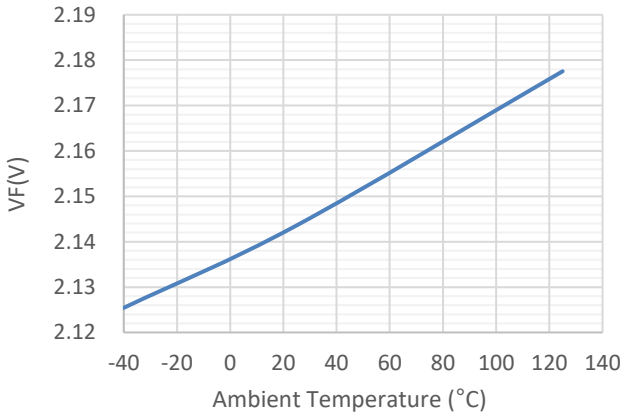


Figure 5.5 Forward voltage drop versus Temperature

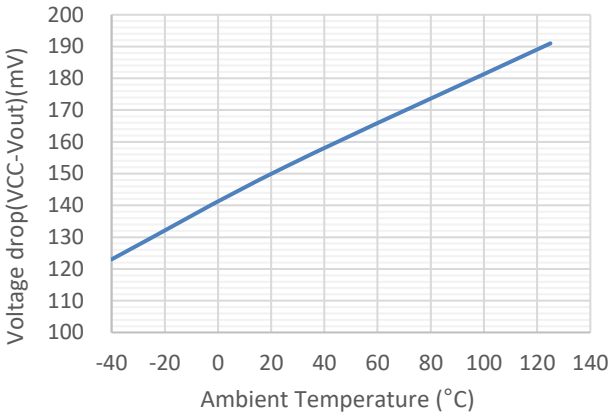


Figure 5.6 V_{OH} (50mA Load) versus Temperature

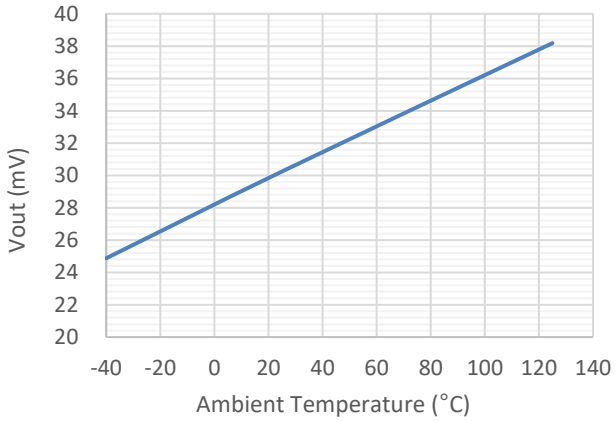


Figure 5.7 V_{OL} versus Temperature

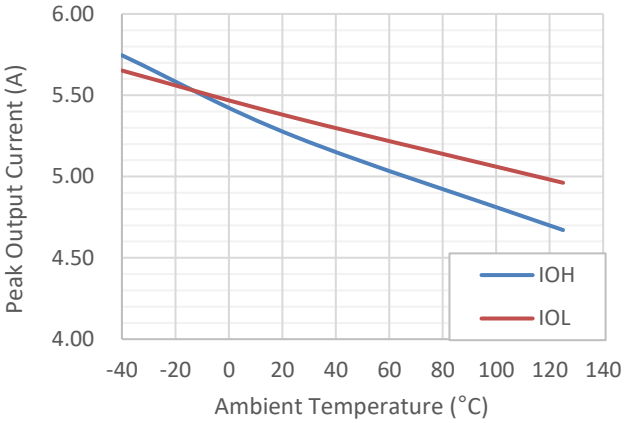


Figure 5.8 Output drive currents versus Temperature

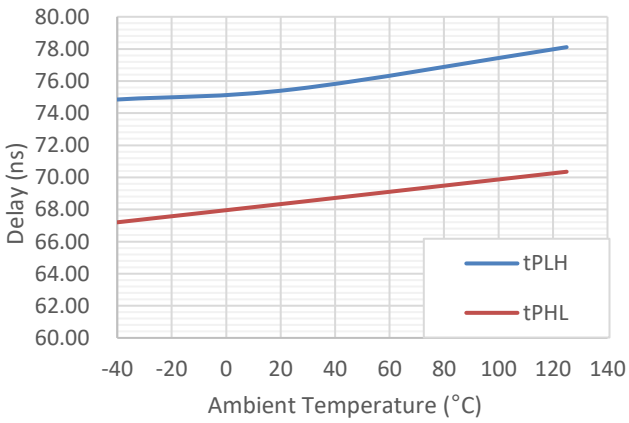


Figure 5.9 Propagation delay versus Temperature

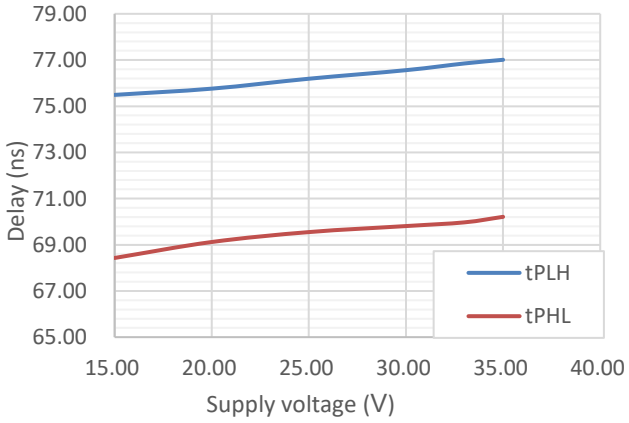


Figure 5.10 Propagation delay versus Supply voltage

5.4. Parameter Measurement Information

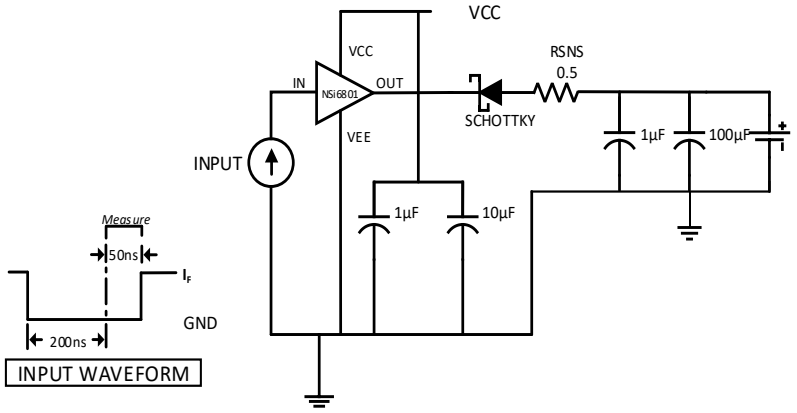


Figure 5.11 I_{OL} Sink Current Test Circuit

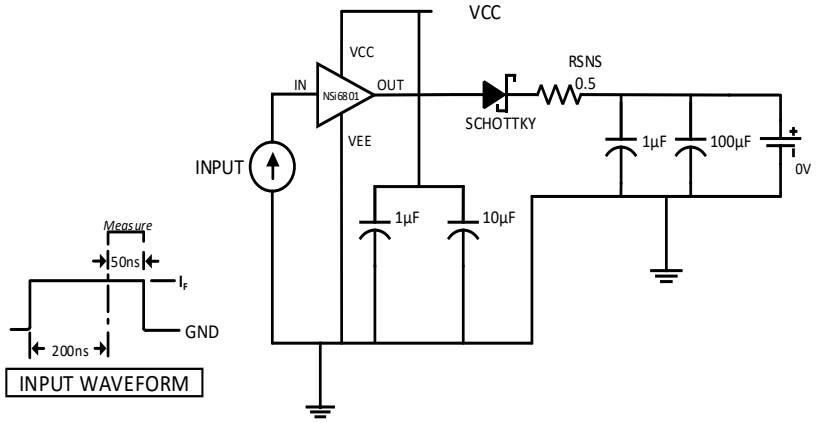


Figure 5.12 I_{OH} Source Current Test Circuit

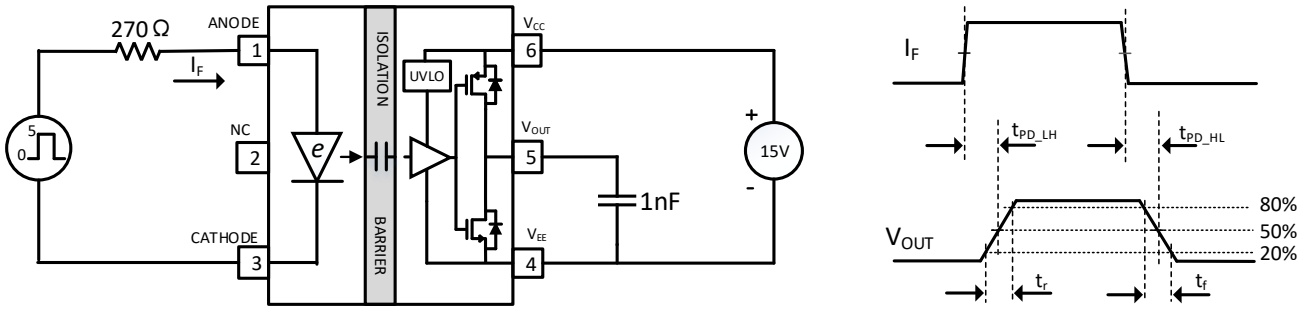


Figure 5.13 I_F to V_{OUT} Propagation Delay, Rise Time and Fall Time

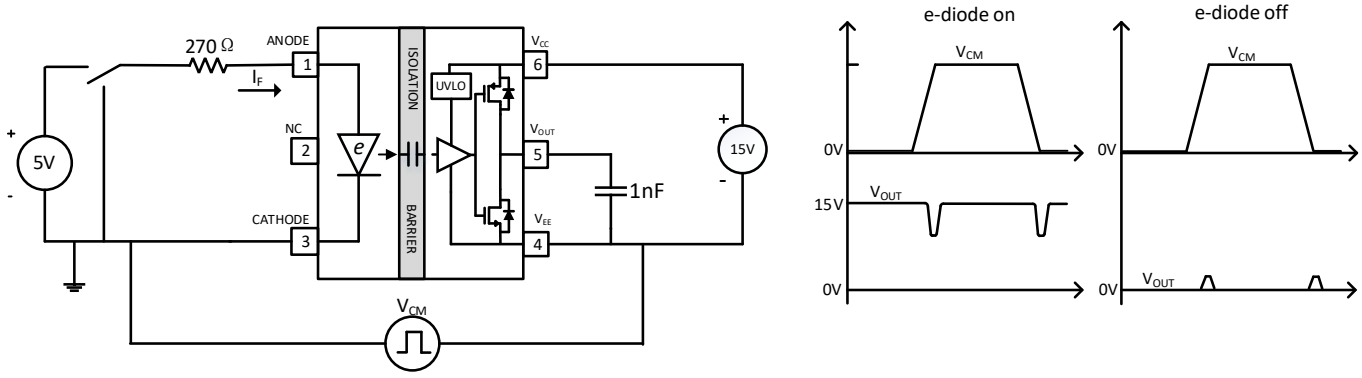


Figure 5.14 Common Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*		*Unit*	*Comments*
		SOW6	*DUB8*		
Minimum External Air Gap (Clearance)	CLR	8	6.5	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8	6.5	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	20		um	Minimum internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	>400	>400	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		II	II		

6.2. DIN VDE V 0884-11 (VDE V 0884-11): 2017-01 Insulation Characteristics for SOW6 Package

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Overvoltage Category	For Rated Mains Voltage ≤ 600V_{RMS}		Ⅰ to Ⅳ	
	For Rated Mains Voltage ≤ 1000V_{RMS}		Ⅰ to Ⅲ	
Climatic Category			40/125/21	
Pollution Degree			2	
Maximum Working Isolation Voltage		V_{IOWM}	1500	V_{RMS}
			2121	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	2121	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{pd(m)}$=V_{IORM}×1.875, 100% production test, t_{ini}=t_m=1s, partial discharge<5pC	$V_{pd(m)}$	3977	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{pd(m)}$=V_{IORM}×1.6, t_{ini}=60s, t_m=10s, partial discharge <5pC	$V_{pd(m)}$	3394	V_{PEAK}
After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{pd(m)}$=V_{IORM}×1.2, t_{ini}=60s, t_m=10s, partial discharge <5pC	$V_{pd(m)}$	2545	V_{PEAK}
Maximum Transient Isolation Voltage	t = 60 s	V_{IOTM}	8000	V_{PEAK}
Maximum Withstanding Isolation Voltage	V_{TEST}= V_{ISO}, t = 60 s (qualification); V_{TEST}= 1.2 ×V_{ISO}, t = 1 s (100%production)	V_{ISO}	5700	V_{RMS}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, V_{TEST}=V_{IOSM}×1.6	V_{IOSM}	6250	V_{PEAK}
Isolation Resistance	V_{IO} =500V at T_A=T_S=150°C	R_{IO}	>10^9	Ω
	V_{IO} =500V at 100°C≤T_A≤125°C		>10^{11}	Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1	pF

6.3. Safety-Limiting Values for SOW6 Package

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Maximum Safety Temperature		T_S	150	°C
Safety Input, Output, or Total Power	$R_{\theta JA}$=125°C/W, T_J=150°C, T_A=25°C	P_S	750	mW
Safety Input, Output, or Supply Current	$R_{\theta JA}$=125°C/W, V_{CC}=15V, T_J=150°C, T_A=25°C	I_S	50	mA
	$R_{\theta JA}$=125°C/W, V_{CC}=30V, T_J=150°C, T_A=25°C	I_S	25	mA

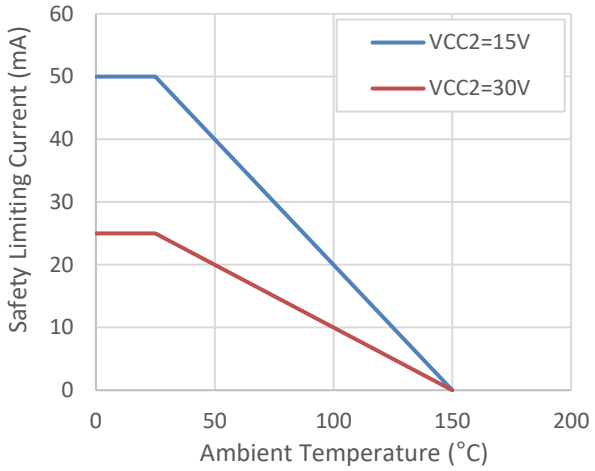


Figure 6.1 Thermal Derating Curve for Limiting Current per DIN VDE V 0884-11 for SOW6 Package

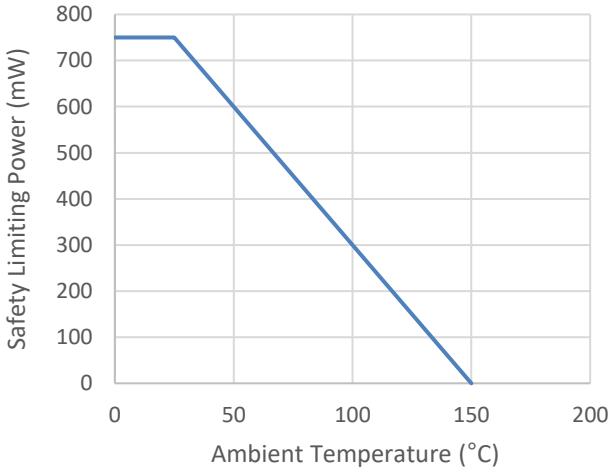


Figure 6.2 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-11 for SOW6 Package

6.4. Regulatory Information for SOW6 Package

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, $5700V_{RMS}$ Isolation Voltage	Single Protection, $5700V_{RMS}$ Isolation voltage	Reinforced Insulation $V_{IORM}=2121V_{PEAK}$, $V_{IOTM}=8000V_{PEAK}$, $V_{IOSM}=6250V_{PEAK}$	Reinforced Insulation
E500602	File (pending)	File (pending)	CQC21001289930

6.5. DIN VDE V 0884-11 (VDE V 0884-11): 2017-01 Insulation Characteristics for DUB8 Package

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Overvoltage Category	For Rated Mains Voltage ≤ 600V_{RMS}		I to IV	
	For Rated Mains Voltage ≤ 1000V_{RMS}		I to III	
Climatic Category			40/125/21	
Pollution Degree			2	
Maximum Working Isolation Voltage		V_{IOWM}	1000	V_{RMS}
			1414	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	1414	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{pd(m)}$=V_{IORM}×1.875, 100% production test, t_{ini}=t_m=1s, partial discharge<5pC	$V_{pd(m)}$	2652	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{pd(m)}$=V_{IORM}×1.6, t_{ini}=60s, t_m=10s, partial discharge <5pC	$V_{pd(m)}$	2263	V_{PEAK}
After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{pd(m)}$=V_{IORM}×1.2, t_{ini}=60s, t_m=10s, partial discharge <5pC	$V_{pd(m)}$	1697	V_{PEAK}
Maximum Transient Isolation Voltage	t = 60 s	V_{IOTM}	8000	V_{PEAK}
Maximum Withstanding Isolation Voltage	V_{TEST}= V_{ISO}, t = 60 s (qualification); V_{TEST}= 1.2 ×V_{ISO}, t = 1 s (100%production)	V_{ISO}	5000	V_{RMS}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, V_{TEST}=V_{IOSM}×1.6	V_{IOSM}	6250	V_{PEAK}
Isolation Resistance	V_{IO} =500V at T_A=T_S=150°C	R_{IO}	>10^9	Ω
	V_{IO} =500V at 100°C≤T_A≤125°C		>10^{11}	Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1	pF

6.6. Safety Limiting Values for DUB8 Package

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Maximum Safety Temperature		T_S	150	°C
Safety Input, Output, or Total Power	$R_{\theta JA}$=125°C/W, T_J=150°C, T_A=25°C	P_S	750	mW
Safety Input, Output, or Supply Current	$R_{\theta JA}$=125°C/W, V_{CC}=15V, T_J=150°C, T_A=25°C	I_S	50	mA
	$R_{\theta JA}$=125°C/W, V_{CC}=30V, T_J=150°C, T_A=25°C	I_S	25	mA

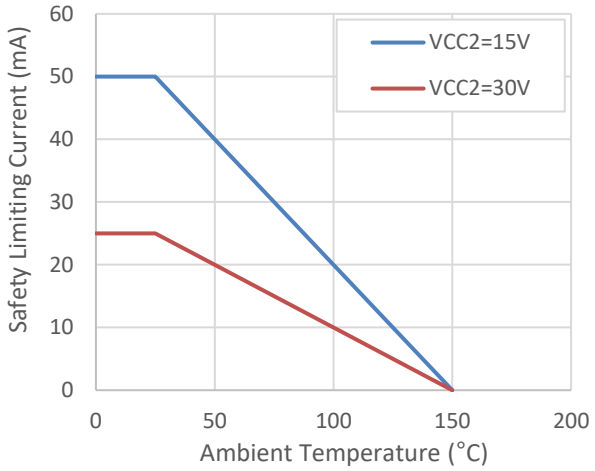


Figure 6.3 Thermal Derating Curve for Limiting Current per DIN VDE V 0884-11 for DUB8 Package

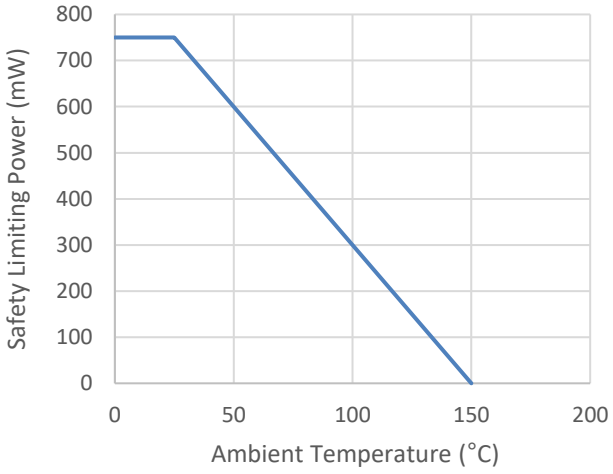


Figure 6.4 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-11 for DUB8 Package

6.7. Regulatory Information for DUB8 Package

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, $5000V_{RMS}$ Isolation Voltage	Single Protection, $5000V_{RMS}$ Isolation voltage	Reinforced Insulation $V_{IORM}=1414V_{PEAK}$, $V_{IOTM}=8000V_{PEAK}$, $V_{IOSM}=6250V_{PEAK}$	Reinforced Insulation
File (pending)	File (pending)	File (pending)	File (pending)

7. Function Description

The NSi6801 is a single-channel isolated gate driver which is pin-compatible for popular opto-coupled gate driver. The integrated galvanic isolation between control input logic and driving output stage grants additional safety. The device can source 5A and sink 5A peak current, which can drive IGBTs, power MOSFETs and SiC MOSFETs in many applications such as motor control systems, solar inverters and power supplies.

7.1. Functional Block Diagram

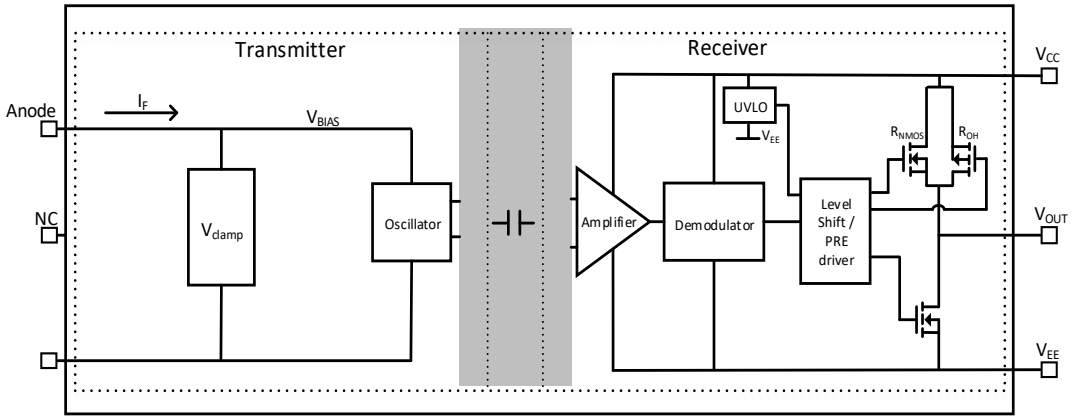


Figure 7.1 NSi6801 Functional Block Diagram

7.2. Truth Tables

Table 7.1 Driver Function Table (1)

e-diode	*V_{CC} status*	*Outputs*
X	Powered Down	L
$I_F>I_{FLH}$	Powered Up	H
$V_F<V_{FHL}$	Powered Up	L

(1) H= Logic High; L= Logic Low; X= Irrelevant

7.3. Output Stage

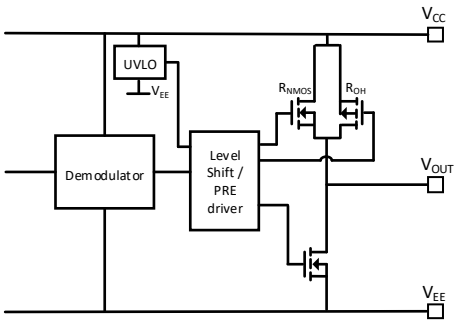


Figure 7.2 NSi6801 Output Stage

Table 7.2 NSi6801 Output Stage On-Resistance

R_{NMOS}	*R_{OH}*	*R_{OL}*	*Unit*
0.8	3	0.6	Ω

The NSi6801 has P-channel and N-channel MOSFET in parallel to pull up the OUT pin when turning on external power transistor. During

DC measurement, only the P-channel MOSFET is conducting. The measurement result R_{OH} represents the on-resistance of P-channel MOSFET.

The voltage and current of external power transistor drain to source or collector to emitter change during turn on. At that time, the NSi6801 N-channel MOSFET turns on to pull up OUT more quickly. It results external power transistor faster turn on time, lower turn on power loss, also leads to smaller temperature increase of NSi6801. The equivalent pull-up resistance of NSi6801 is the parallel combination ROH || RNMOS. The result is quite small, indicating the strong driving capability of NSi6801.

The pull-down structure of NSi6801 is simply composed of an N-channel MOSFET with on-resistance of R_{OL}. The result is quite small, indicating the strong driving capability of NSi6801.

7.4. V_{CC} and Under Voltage Lock Out (UVLO)

The lower limit of driver side supply voltage (V_{CC}) is determined by the internal UVLO protection feature of the device. V_{CC} voltage should not fall below the UVLO threshold for normal operation, or else the gate-driver outputs can become clamped low.

A local bypass capacitor should be placed between the V_{CC} and V_{EE} pins, with a value of 220-nF to 10-µF for device biasing. An additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended.

7.5. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if V_{CC} is not connected to the power supply. When V_{CC} is floating, the driver output is held low and clamping V_{OUT} pin to approximately 1.9V higher than V_{EE}.

7.6. Short Circuit Clamping

During short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the Miller capacitance. The diode between V_{OUT} and V_{CC} pins inside the driver limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500 mA may be fed back to the supply through this path for 10 µs. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

8. Application Note

8.1. Typical Application

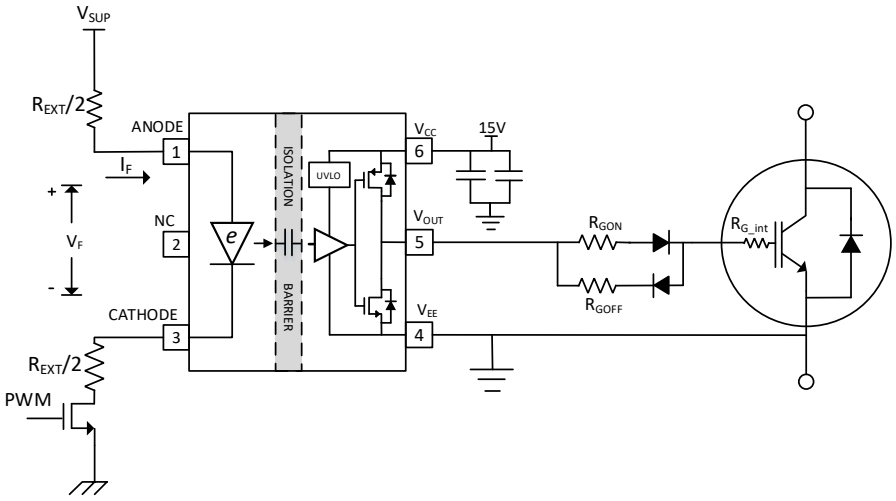


Figure 8.1 NSi6801 typical application circuit with NMOS driving input stage

Bypassing capacitors connecting between V_{CC} and V_{EE} are needed to achieve reliable performance. To filter noise, 0.1μF/50V ceramic capacitor is recommended to place as close as possible to NSi6801. To support high peak currents when turning on external power transistor, additional 10μF/50V ceramic capacitor is recommended. If the V_{CC} power supply is located long distance from the IC, bigger capacitance is needed.

NSi6801 requires 7mA to 16mA bias current that flows into the e-diode for normal operation. The PWM from MCU is not suitable to provide such current directly and external circuit is needed. In Figure 8.1, one NMOS is used with split input resistors. Another input drive method is using one buffer, as shown in Figure 8.2. The details to calculate input drive parameters are in Chapter 8.3.

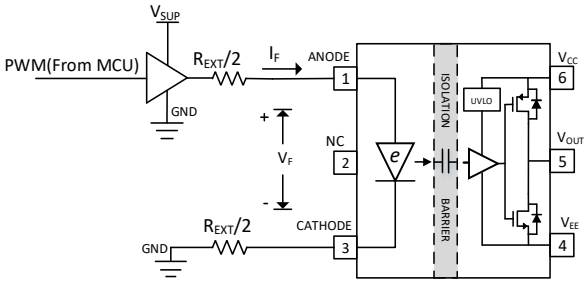


Figure 8.2 NSi6801 typical application circuit with one buffer driving input stage

8.2. Interlock Protection

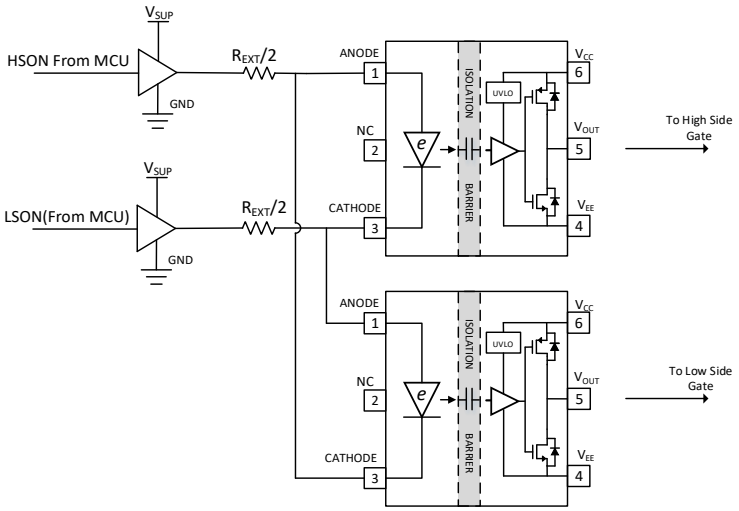


Figure 8.3 Interlock Protection using NSi6801

For applications to drive power transistors in half bridge configuration, two NSi6801 can be used. Interlock protection is possible as shown in Figure 5.3. If the controller has some mistake, leading to negative dead time, the output PWM of NSi6801 is adjusted to avoid power transistor shoot through. The input side reverse breakdown voltage of NSi6801 is greater than 6.5V, which supports interlock protection of 3.3V or 5V PWM signal source.

8.3. Selecting Input Resistor

The recommended forward current range for NSi6801 is 7mA to 16mA. The value of input resistor, buffer supply voltage and buffer internal resistance influence the forward current, as shown in Equation (1). In Figure 8.1, R_{Buffer} is the on-resistance of the external NMOS. In Figure 8.2, R_{Buffer} is the buffer output impedance in output "High" state. In Figure 8.3, R_{Buffer} is the summary of buffer output impedance in "High" and "Low" state.

$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{Buffer} \quad (1)$$

The parameter variation needs to be taken into consideration when selecting input resistor. Table 8.1 lists parameter variation in this example. The corresponding external resistor calculation result is 196Ω min, 262Ω typ and 300Ω max.

Table 8.1 External parameters range when calculating input resistor

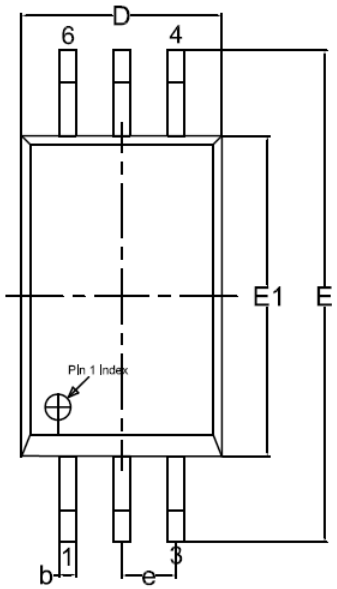
Parameters	*Min*	*Typ*	*Max*
NSi6801 forward current I_F	7mA	10mA	16mA
NSi6801 forward voltage V_F	1.8V	2.1V	2.4V
Buffer supply voltage V_{SUP}	5V*95%	5V	5V*105%
Buffer internal resistance R_{Buffer}	13Ω	18Ω	22Ω

8.4. PCB Layout

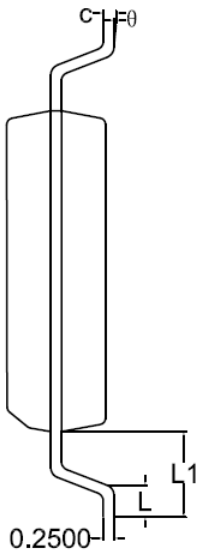
Carful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSi6801, between V_{CC} to V_{EE}.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSi6801 close to power transistor.
- Place large amount of copper connecting to V_{EE} pin and V_{CC} pin for thermal dissipation, with priority on V_{EE} pin. If the system has multi V_{EE} or V_{CC} layers, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

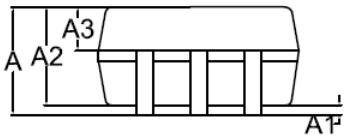
9. Package Information



TOP VIEW



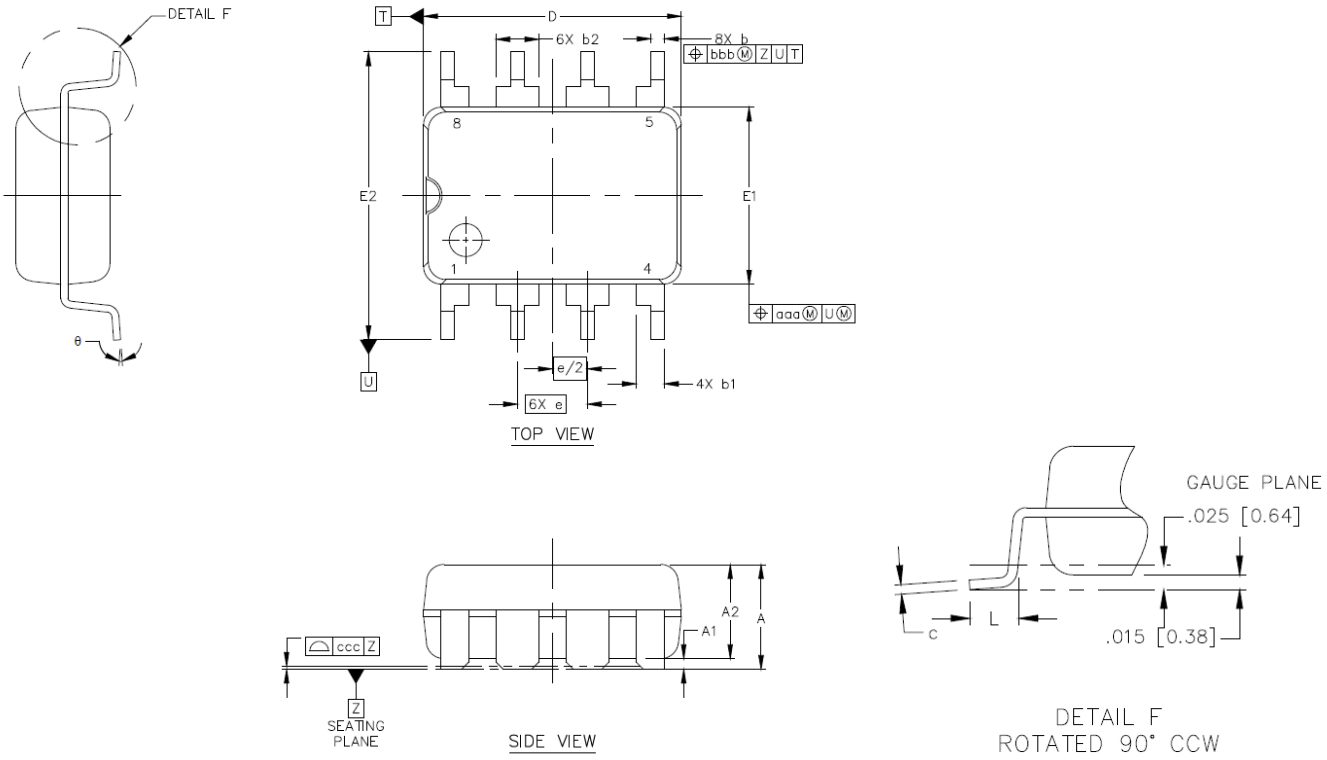
SIDE VIEW



SIDE VIEW

	DIMENSIONS IN MILLIMETERS		
REF.	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
E	11.25	11.50	11.75
E1	7.40	7.50	7.60
D	4.58	4.68	4.78
L	0.50	—	1.00
b	0.28	—	0.51
c	0.25	—	0.29
θ	0°	—	8°
e	1.27 BSC		
L1	2.00 BSC		

Figure 9.1 SOW6 Package Shape and Dimension in millimeters



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	3.58	---	4.19
STAND OFF	A1	0.38	---	0.58
MOLD THICKNESS	A2	3.20	---	3.61
LEAD WIDTH	b	0.36	---	0.56
	b1	---	0.99 REF	---
	b2	---	1.524 REF	--
L/F THICKNESS	c	0.20	---	0.36
BODY SIZE	D	9.27	---	9.37
	E1	6.20	---	6.60
	E2	10.11	---	10.69
LEAD PITCH	e	2.54 BSC		
LEAD LENGTH	L	1.15	---	1.45
	θ	0°	---	8°
LEAD OFFSET	aaa	0.254		

Figure 9.2 DUB8 Package Shape and Dimension in millimeters

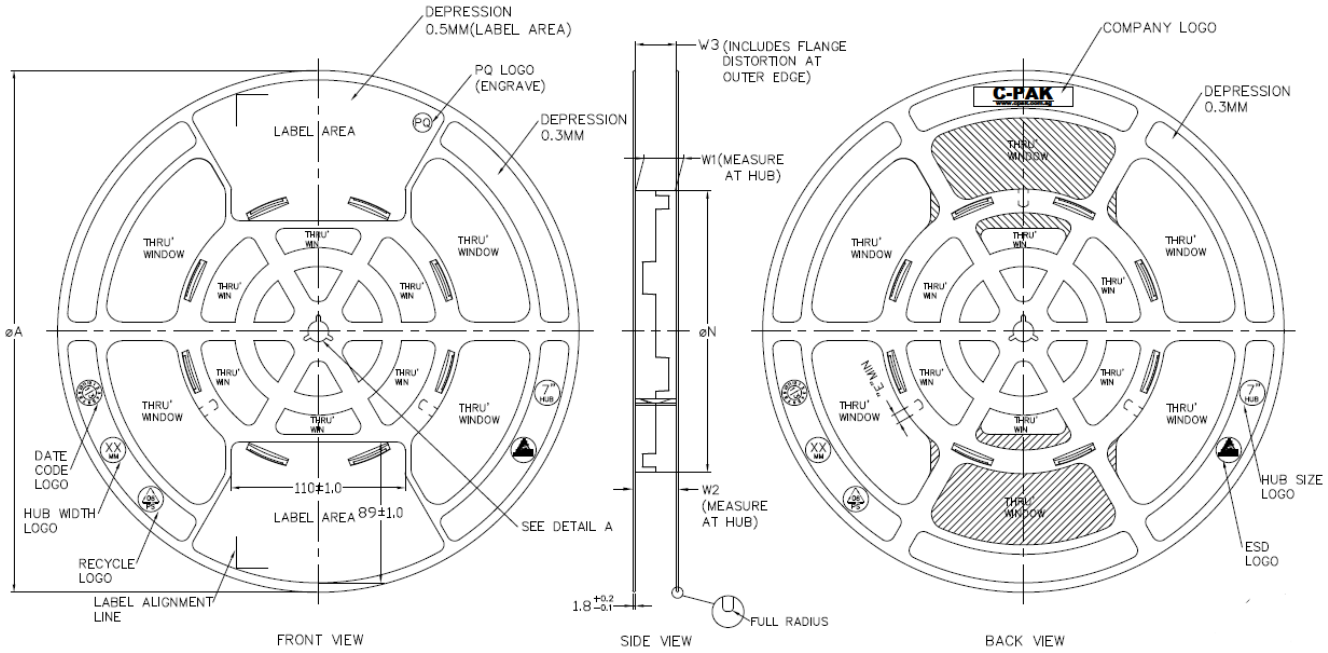
10. Ordering Information

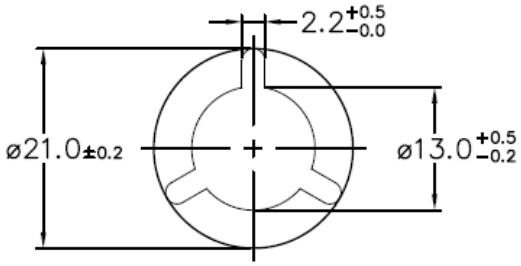
Part Number	*Isolation Rating (kV)*	*UVLO Level*	*Vout Connection*	*Temperature*	*MSL*	*Package Drawing*	*SPQ*
NSi6801B-DSWFR	5.7	9V	Pin 5	-40 to 125°C	3	SOW6	1000
NSi6801C-DSWFR	5.7	13V	Pin 5	-40 to 125°C	3	SOW6	1000
NSi6801TB-DDBR	5	9V	Pin 6, 7	-40 to 125°C	3	DUB8	800
NSi6801TC-DDBR	5	13V	Pin 6, 7	-40 to 125°C	3	DUB8	800
NSi6801LC-DDBR	5	13V	Pin 6	-40 to 125°C	3	DUB8	800

11. Documentation Support

Part Number	***Product Folder***	***Datasheet***	***Technical Documents***	***Isolated Driver Selection Guide***
NSi6801	Click here	Click here	Click here	Click here

12. Tape and Reel Information



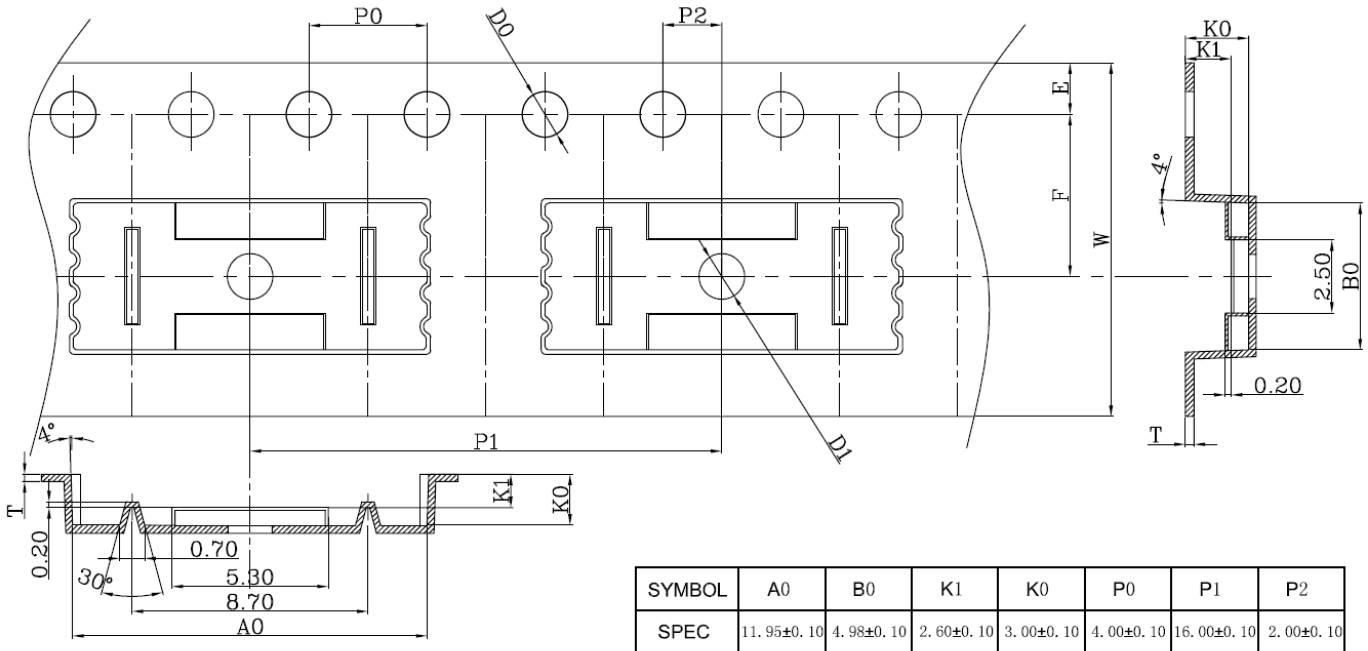


ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

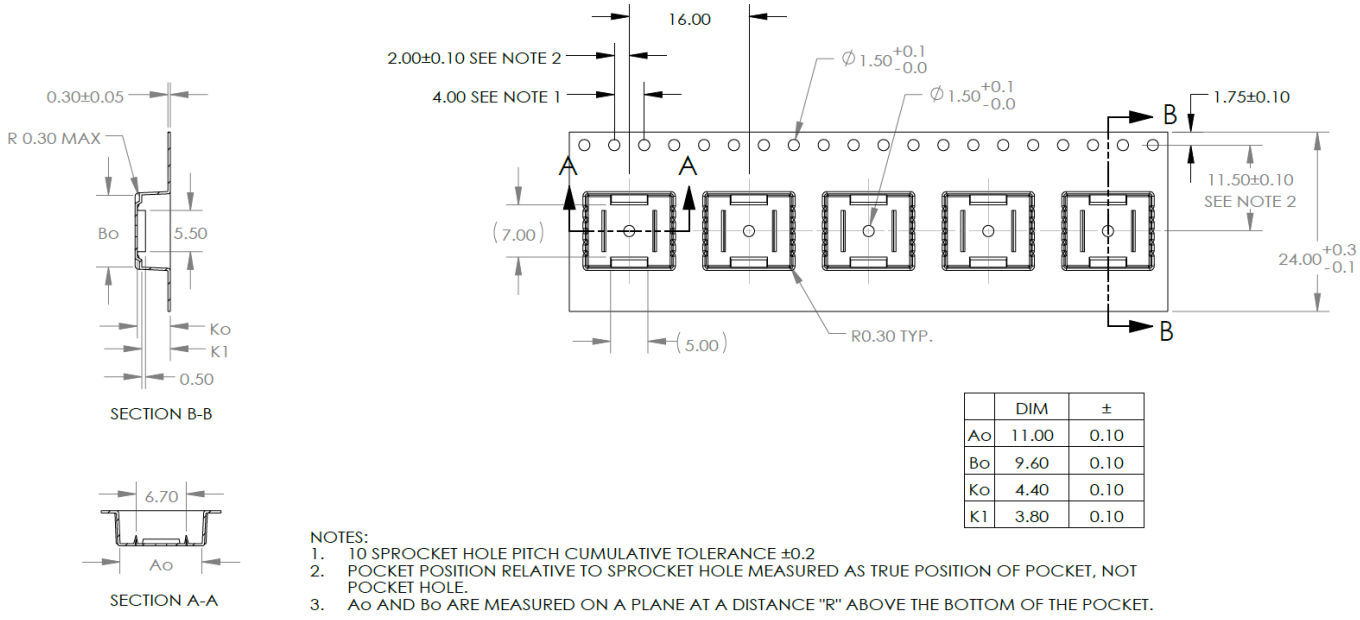
SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 12.1 Tape Information



SYMBOL	A0	B0	K1	K0	P0	P1	P2
SPEC	11.95±0.10	4.98±0.10	2.60±0.10	3.00±0.10	4.00±0.10	16.00±0.10	2.00±0.10
SYMBOL	T	E	F	D0	D1	W	
SPEC	0.30±0.03	1.75±0.10	7.50±0.05	1.55±0.05	1.55±0.10	$16.0^{+0.30}_{-0.10}$	

Figure 12.2 Reel Information of SOW6



	DIM	±
Ao	11.00	0.10
Bo	9.60	0.10
Ko	4.40	0.10
K1	3.80	0.10

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 12.3 Reel Information of DUB8

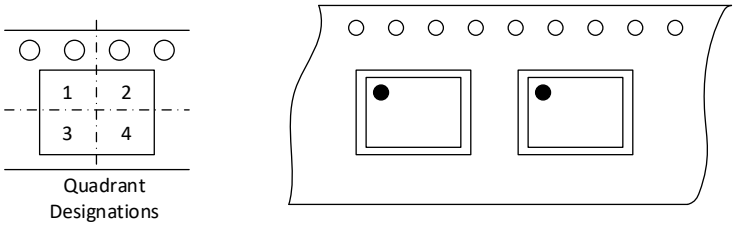


Figure 12.4 Quadrant Designation for Pin1 Orientation in Tape

13. Reversion History

Revision	Description	Date
1.0	Initial version	2021/4/16