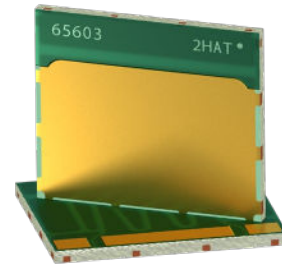


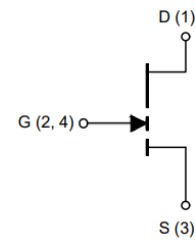
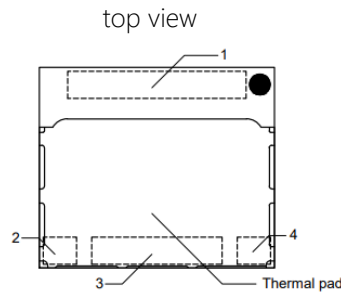
### Features

- 650 V enhancement mode power transistor
- Top-cooled, low inductance GaN<sub>Px</sub>® package
- $R_{DS(on)} = 25 \text{ m}\Omega$
- $I_{DS(max)} = 60 \text{ A}$
- Ultra-low FOM
- Simple drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 / +10 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Reverse conduction capability
- Zero reverse recovery loss
- Small 9.2 x 7.8 mm<sup>2</sup> footprint
- Dual gate pads for optimal board layout
- RoHS 3 (6+4) compliant



Package Outline

Circuit Symbol



The thermal pad is internally connected to Source (pin 3) and substrate.

### Applications

- AC-DC Converters
- DC-DC Converters
- Bridgeless Totem Pole PFC
- Inverters
- Energy Storage Systems
- On Board Battery Chargers
- Uninterruptable Power Supplies
- Solar Energy
- Industrial Motor Drives
- Laser Drivers
- Traction Drive
- Wireless Power Transfer

### Description

The GS-065-060-3-T is an enhancement mode GaN-on-Silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems innovates with industry leading advancements such as patented **Island Technology**® and **GaN<sub>Px</sub>**® packaging. **Island Technology**® cell layout realizes high-current die and high yield. **GaN<sub>Px</sub>**® packaging enables low inductance & low thermal resistance in a small package. The GS-065-060-3-T is a top-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

### Absolute Maximum Ratings ( $T_{case} = 25\text{ °C}$ except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	$T_J$	-55 to +150	°C
Storage Temperature Range	$T_S$	-55 to +150	°C
Drain-to-Source Voltage	$V_{DS}$	650	V
Transient Drain-to-Source Voltage (Note 1)	$V_{DS(transient)}$	900	V
Gate-to-Source Voltage	$V_{GS}$	-10 to +7	V
Gate-to-Source Voltage - transient (Note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current ( $T_{case}=25\text{ °C}$ )	$I_{DS}$	60	A
Continuous Drain Current ( $T_{case}=100\text{ °C}$ )	$I_{DS}$	47	A
Pulse Drain Current (Pulse width 50 $\mu$ s, $V_{GS} = 6\text{ V}$ ) (Note 2)	$I_{DS\ Pulse}$	120	A

(1) For  $\leq 1\ \mu$ s

(2) Defined by product design and characterization. Value is not tested to full current in production.

### Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – top side	$R_{\theta JC}$	0.27	°C /W
Maximum Soldering Temperature (MSL3 rated)	$T_{SOLD}$	260	°C

### Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
GS-065-060-3-T-TR	GaN $Px$ ® Top-Side Cooled	Tape-and-Reel	3000	13" (330 mm)	16mm
GS-065-060-3-T-MR	GaN $Px$ ® Top-Side Cooled	Mini-Reel	250	7" (180 mm)	16mm

**Electrical Characteristics** (Typical values at  $T_J = 25\text{ }^\circ\text{C}$ ,  $V_{GS} = 6\text{ V}$  unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	650			V	$V_{GS} = 0\text{ V}$ , $I_{DSS} \leq 120\text{ }\mu\text{A}$
Drain-to-Source On Resistance	$R_{DS(on)}$		25	32	m $\Omega$	$V_{GS} = 6\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$ $I_{DS} = 18\text{ A}$
Drain-to-Source On Resistance	$R_{DS(on)}$		65		m $\Omega$	$V_{GS} = 6\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ $I_{DS} = 18\text{ A}$
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	$V_{DS} = V_{GS}$ , $I_{DS} = 16.4\text{ mA}$
Gate-to-Source Current	$I_{GS}$		320		$\mu\text{A}$	$V_{GS} = 6\text{ V}$ , $V_{DS} = 0\text{ V}$
Gate Plateau Voltage	$V_{plat}$		3		V	$V_{DS} = 400\text{ V}$ , $I_{DS} = 60\text{ A}$
Drain-to-Source Leakage Current	$I_{DSS}$		4	120	$\mu\text{A}$	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ $T_J = 25\text{ }^\circ\text{C}$
Drain-to-Source Leakage Current	$I_{DSS}$		160		$\mu\text{A}$	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$
Internal Gate Resistance	$R_G$		1		$\Omega$	$f = 5\text{ MHz}$ , open drain
Input Capacitance	$C_{ISS}$		516		pF	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 100\text{ kHz}$
Output Capacitance	$C_{OSS}$		127		pF	
Reverse Transfer Capacitance	$C_{RSS}$		2.4		pF	
Effective Output Capacitance Energy Related (Note 3)	$C_{O(ER)}$		212		pF	$V_{GS} = 0\text{ V}$ $V_{DS} = 0\text{ to }400\text{ V}$
Effective Output Capacitance Time Related (Note 4)	$C_{O(TR)}$		338		pF	
Total Gate Charge	$Q_G$		14		nC	$V_{GS} = 0\text{ to }6\text{ V}$ $V_{DS} = 400\text{ V}$
Gate-to-Source Charge	$Q_{GS}$		3.8		nC	
Gate-to-Drain Charge	$Q_{GD}$		4.1		nC	
Output Charge	$Q_{OSS}$		135		nC	$V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$
Reverse Recovery Charge	$Q_{RR}$		0		nC	

(3)  $C_{O(ER)}$  is the fixed capacitance that would give the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 V to the stated  $V_{DS}$

(4)  $C_{O(TR)}$  is the fixed capacitance that would give the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 V to the stated  $V_{DS}$ .

**Electrical Characteristics cont'd** (Typical values at  $T_J = 25\text{ }^\circ\text{C}$ ,  $V_{GS} = 6\text{ V}$  unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay	$t_{D(on)}$		8.1		ns	$V_{DD} = 400\text{ V}$ , $V_{GS} = +6\text{ V}/-3\text{ V}$ $I_{DS} = 20\text{ A}$ , $R_{G(on)} = 10\ \Omega$ , $R_{G(off)} = 2\ \Omega$ , $L = 65\ \mu\text{H}$ , $L_p = 4\text{ nH}$ (Notes 5,6,7)
Rise Time	$t_R$		8.5		ns	
Turn-Off Delay	$t_{D(off)}$		9.8		ns	
Fall Time	$t_F$		7.7		ns	
Switching Energy during turn-on	$E_{on}$		117		$\mu\text{J}$	
Switching Energy during turn-off	$E_{off}$		17.2		$\mu\text{J}$	
Output Capacitance Stored Energy	$E_{OSS}$		17		$\mu\text{J}$	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$ , $f = 100\text{ kHz}$

(5) See Figure 16 for switching test circuit diagram.

(6) See Figure 17 for switching time definition waveforms.

(7)  $L_p$  = parasitic inductance.

Electrical Performance Graphs

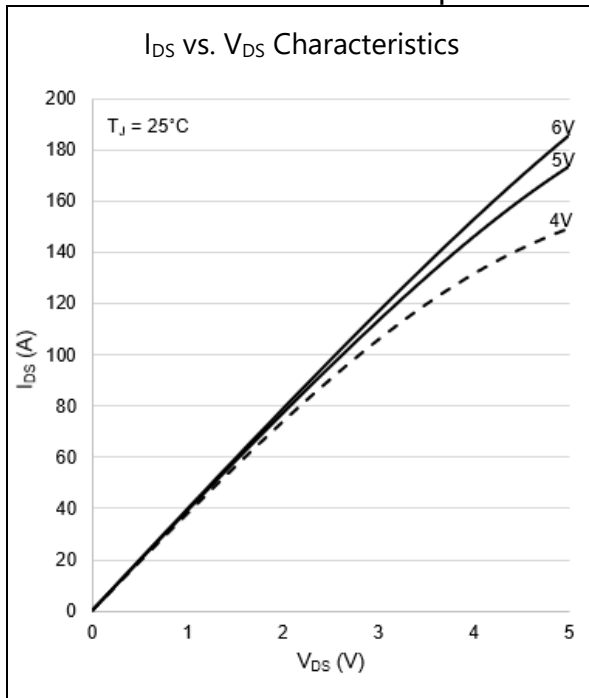


Figure 1: Typical  $I_{DS}$  vs.  $V_{DS}$  @  $T_J = 25^\circ\text{C}$

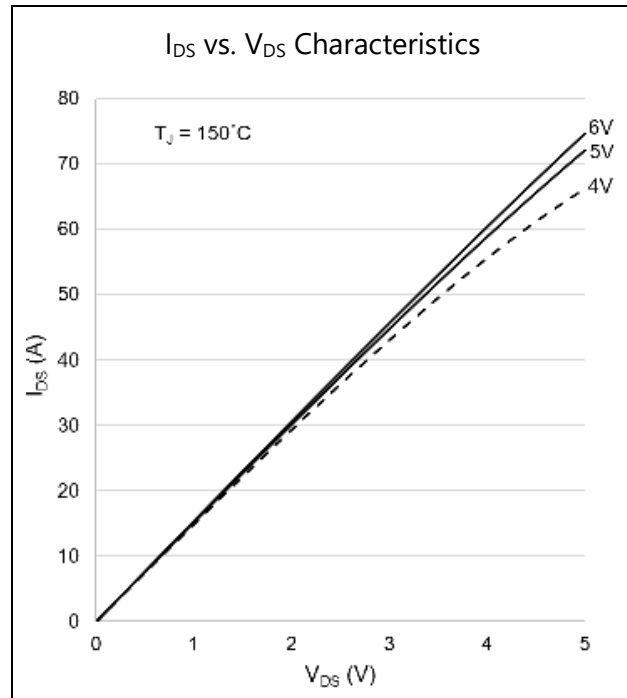


Figure 2: Typical  $I_{DS}$  vs.  $V_{DS}$  @  $T_J = 150^\circ\text{C}$

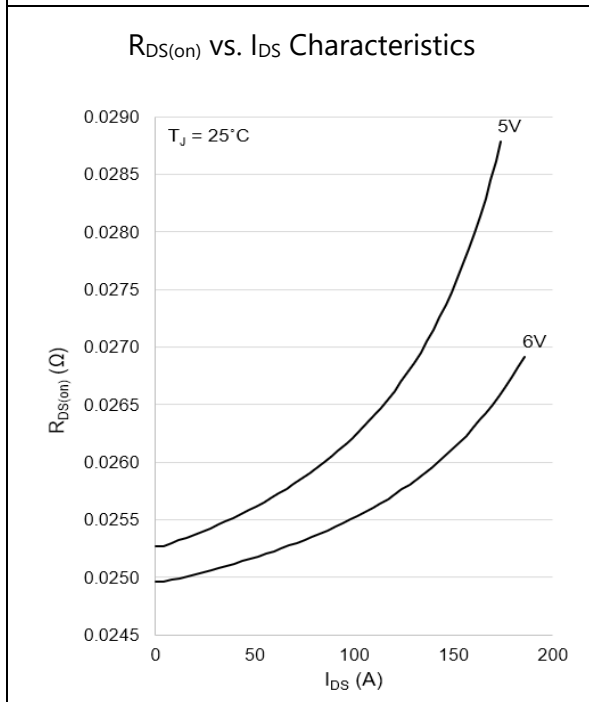


Figure 3:  $R_{DS(on)}$  vs.  $I_{DS}$  at  $T_J = 25^\circ\text{C}$

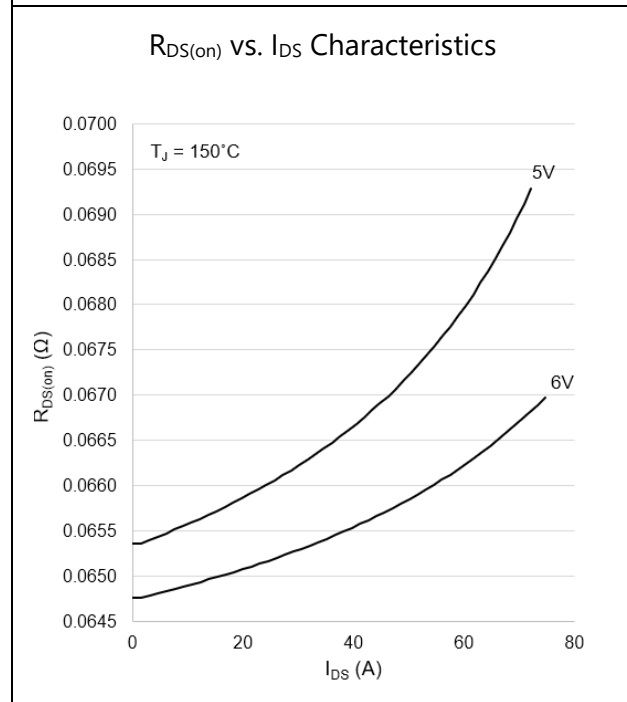


Figure 4:  $R_{DS(on)}$  vs.  $I_{DS}$  at  $T_J = 150^\circ\text{C}$

Electrical Performance Graphs

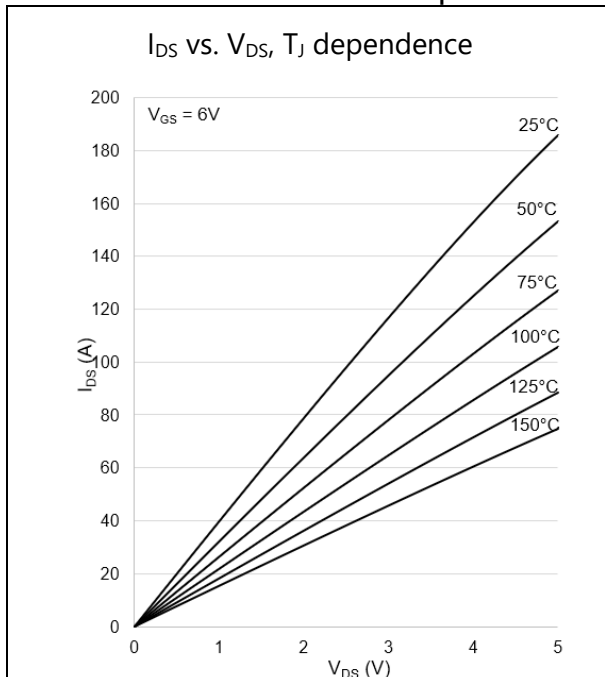


Figure 5: Typical  $I_{DS}$  vs.  $V_{DS}$  @  $V_{GS} = 6\text{ V}$

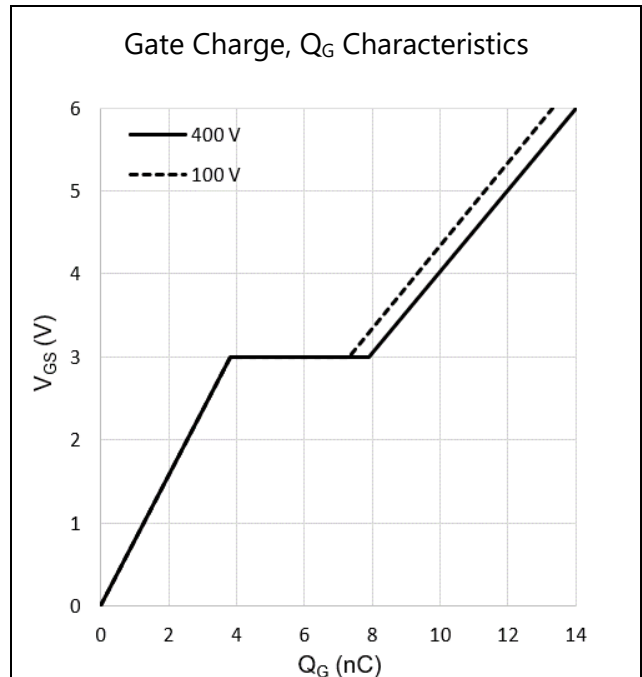


Figure 6: Typical  $V_{GS}$  vs.  $Q_G$  @  $V_{DS} = 100, 400\text{ V}$

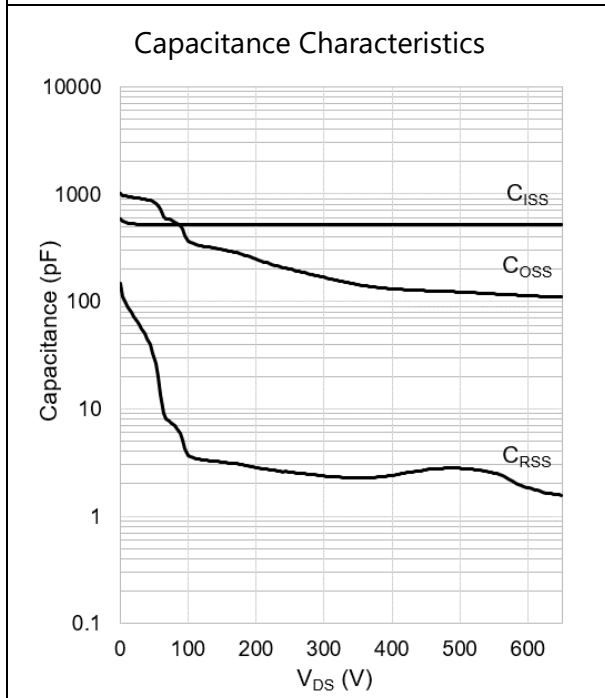


Figure 7: Typical  $C_{ISS}$ ,  $C_{OSS}$ ,  $C_{RSS}$  vs.  $V_{DS}$

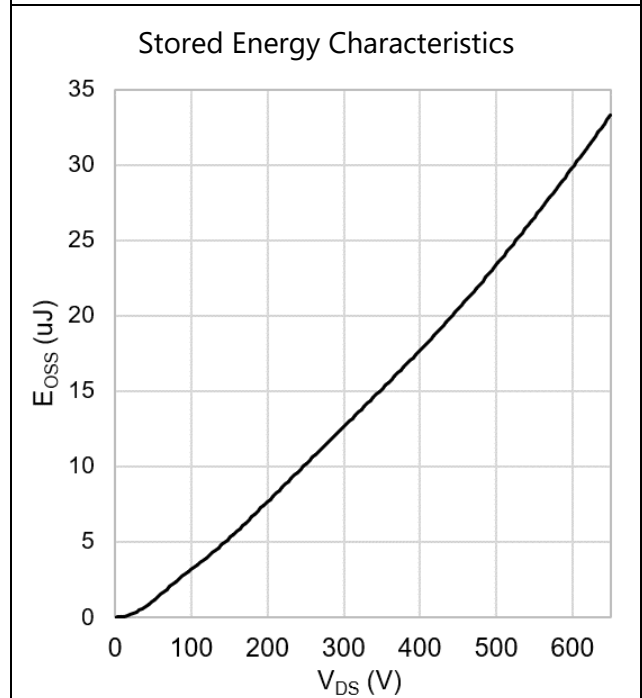
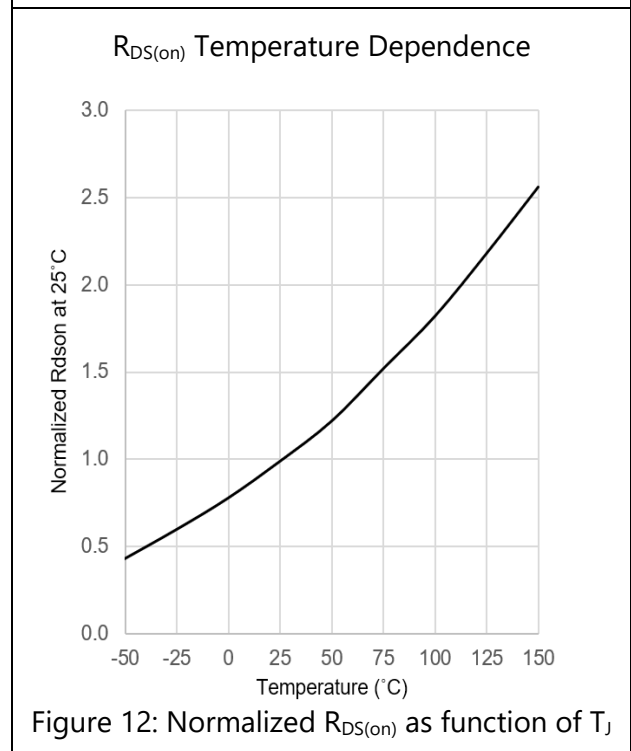
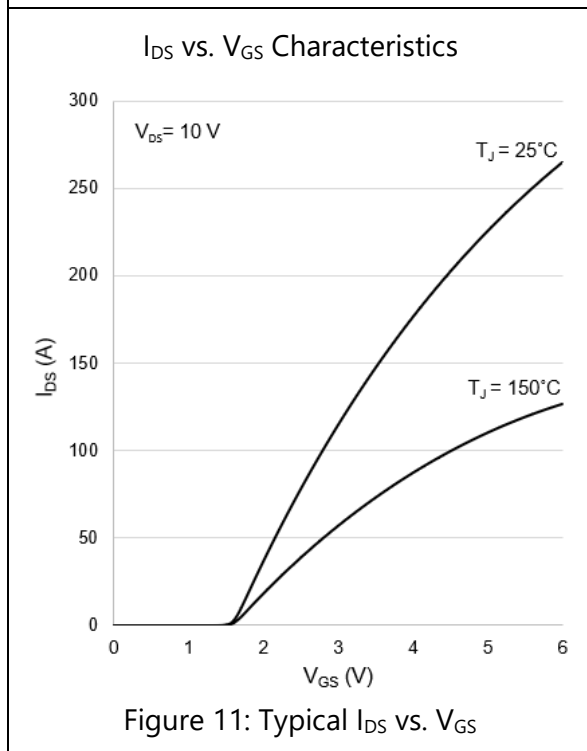
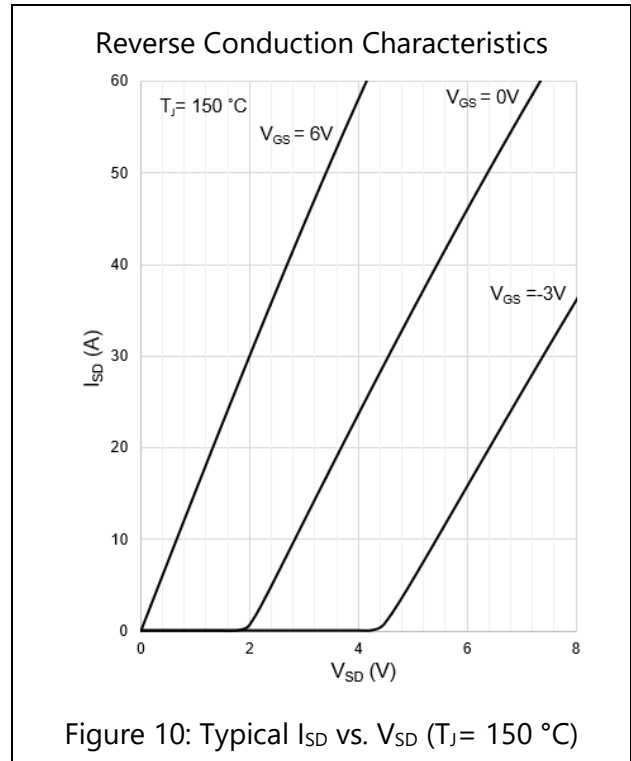
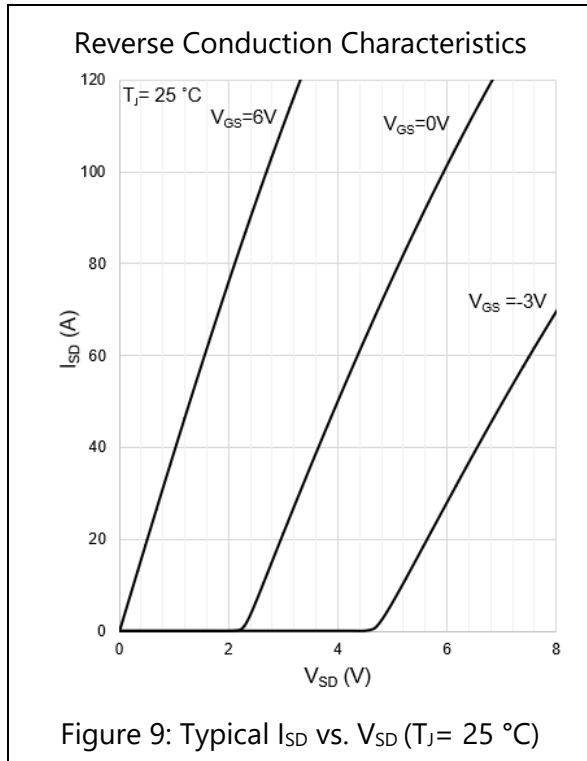


Figure 8: Typical  $C_{OSS}$  Stored Energy

Electrical Performance Graphs



Thermal Performance Graphs

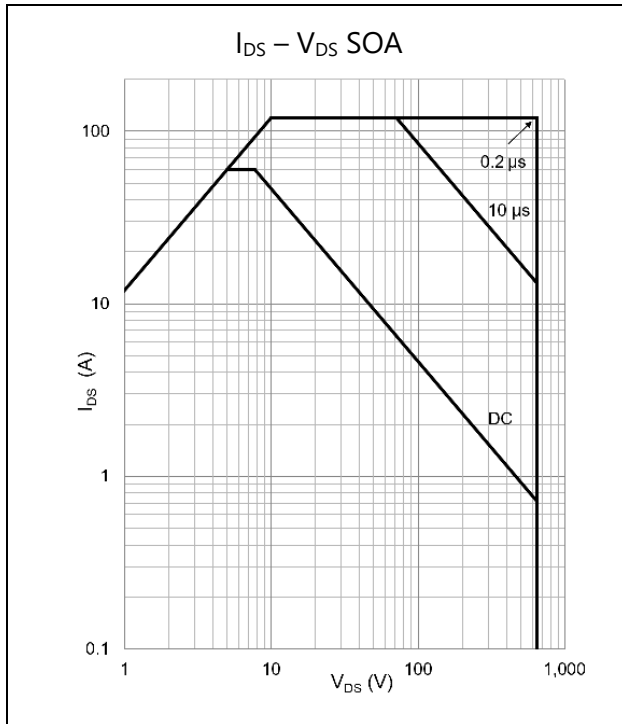


Figure 13: Safe Operating Area @  $T_{case} = 25^\circ C$

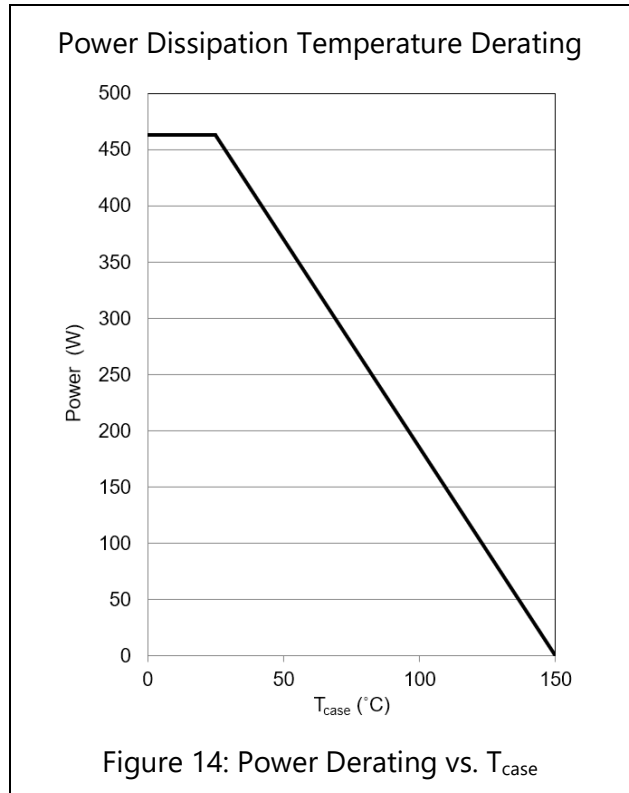


Figure 14: Power Derating vs.  $T_{case}$

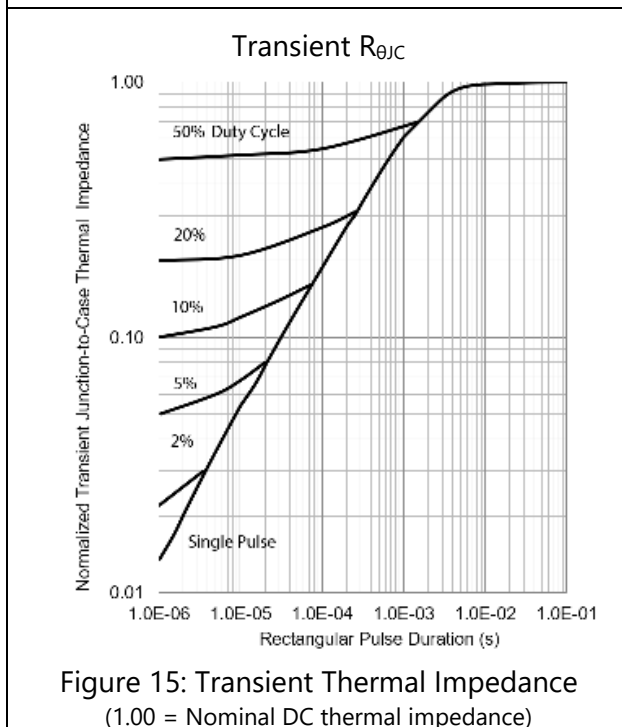


Figure 15: Transient Thermal Impedance  
(1.00 = Nominal DC thermal impedance)



Test Circuits

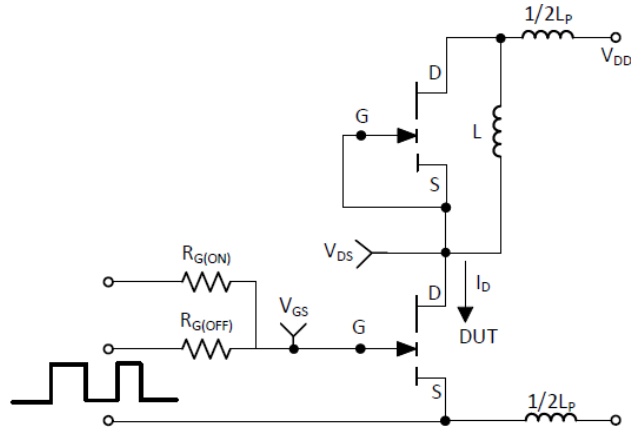


Figure 16: Switching Test Circuit

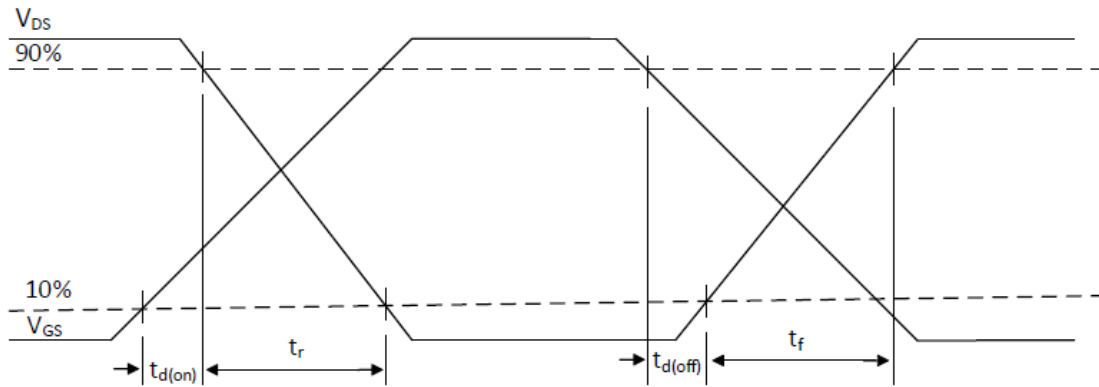


Figure 17: Switching Time Waveforms

## Application Information

For more information, please refer to the application note entitled: "An Introduction to GaN Enhancement Mode HEMTs" at [www.gansystems.com](http://www.gansystems.com)

### Gate Drive

The recommended gate drive voltage range,  $V_{GS}$ , is 0 V to + 6 V for optimal  $R_{DS(on)}$  performance. Also, the repetitive gate to source voltage, maximum rating,  $V_{GS(AC)}$ , is +7 V to -10 V. The gate can survive non-repetitive transients up to +10 V and - 20 V for pulses up to 1  $\mu$ s. These specifications allow designers to easily use 6.0 V or 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias, typically  $V_{GS} = -3$  V, ensures safe operation against the voltage spike on the gate, however it may increase reverse conduction losses if not driven properly. For more details, please refer to the gate driver application note "Gate Driver Circuit Design with GaN E-HEMTs" at [www.gansystems.com](http://www.gansystems.com)

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance,  $R_{G(OFF)}$  is recommended for better immunity to cross conduction. Please see the gate driver application note for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower  $Q_G$  when compared to equally sized  $R_{DS(on)}$  MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive may not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Please see the gate driver application note for more details.

### Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

The dual gate drive pins are used to achieve balanced gate drive, especially useful in parallel GaN transistors operation. Both gate drive pins are internally connected to the gate, so only one needs to be connected. Connecting both may lead to timing improvements at very high frequencies. The two gates on the GS-065-060-3-T top-side cooled device are not designed to be used as a signal pass-through. When multiple devices are used in parallel, it is not recommended to use one gate connection to the other (on the same transistor) as a signal path for the gate drive to the next device. Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2  $\Omega$ ) on each gate is strongly recommended to minimize the gate parasitic oscillation.

### Source Sensing

Although the device does not have a dedicated source sense pin, the GaNPX® packaging utilizes no wire bonds so the source connection is already very low inductance. By simply using a dedicated “source sense” connection on the PCB to the Source pad in a kelvin configuration, the function can easily be implemented. It is recommended to implement a “source sense” connection to improve drive performance.

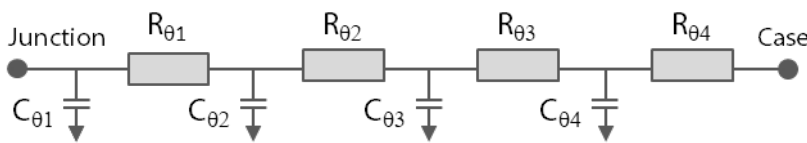
### Thermal

The substrate is internally connected to the thermal pad on the top-side and to the source pin on the bottom side of the package. The transistor is designed to be cooled using a heat sink on the top of the device. The Drain and Source pads are not as thermally conductive as a thermal pad. However, adding more copper under these two pads will improve thermal performance by reducing the packaging temperature.

### Thermal Modeling

RC thermal models are available to support detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This thermal model can be extended to the system level by adding extra  $R_{\theta}$  and  $C_{\theta}$  to simulate the Thermal Interface Material (TIM) or Heatsink.

RC thermal model:



RC breakdown of  $R_{\theta JC}$

$R_{\theta}$ ( $^{\circ}\text{C}/\text{W}$ )	$C_{\theta}$ ( $\text{W}\cdot\text{s}/^{\circ}\text{C}$ )
$R_{\theta 1} = 0.008$	$C_{\theta 1} = 0.2\text{E-}03$
$R_{\theta 2} = 0.08$	$C_{\theta 2} = 1.2\text{E-}03$
$R_{\theta 3} = 0.142$	$C_{\theta 3} = 8.5\text{E-}03$
$R_{\theta 4} = 0.04$	$C_{\theta 4} = 3.7\text{E-}03$

For more detail, please refer to Application Note entitled “Modeling Thermal Behavior of GaN Systems’ GaNPX® Using RC Thermal SPICE Models” available at [www.gansystems.com](http://www.gansystems.com)

### Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition ( $V_{GS} = +6$  V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance,  $R_{DS(on)}$ , similar to forward conduction operation.

Off-state condition ( $V_{GS} \leq 0$  V): The reverse characteristics in the off-state are different from silicon MOSFET as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, ( $V_{GD}$ ) exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a “body diode” with slightly higher  $V_F$  and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than  $V_{GS(th)} + V_{GS(off)}$  in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop “ $V_F$ ” and hence increase the reverse conduction loss.

### Blocking Voltage

The blocking voltage rating,  $V_{(BL)DSS}$ , is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30% higher than the rated  $V_{(BL)DSS}$ . As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and does not change with negative gate voltage. GaN Systems tests devices in production with a 900 V Drain-to-source voltage pulse to insure blocking voltage margin.

### Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

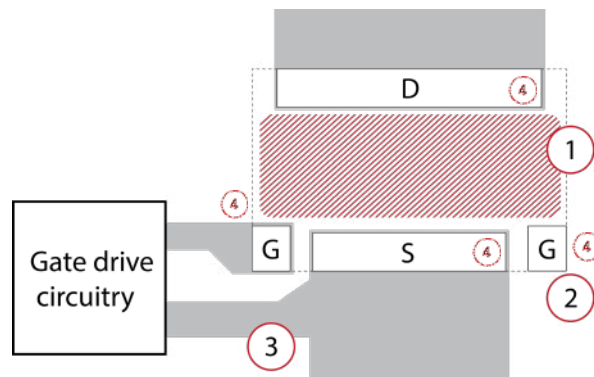
- Preheat/Soak: 60-120 seconds.  $T_{min} = 150$  °C,  $T_{max} = 200$  °C.
- Reflow: Ramp up rate 3°C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using “No-Clean” soldering paste and operating at high temperatures may cause a reactivation of the “No-Clean” flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the “No-Clean” paste residues.

Avoid placing printed circuit board traces with high differential voltage to the source or drain directly underneath the top-cooled GS-065-060-3-T package on the PCB to avoid potential electro-migration and solder mask isolation issues during high temperature or/and voltage operation.

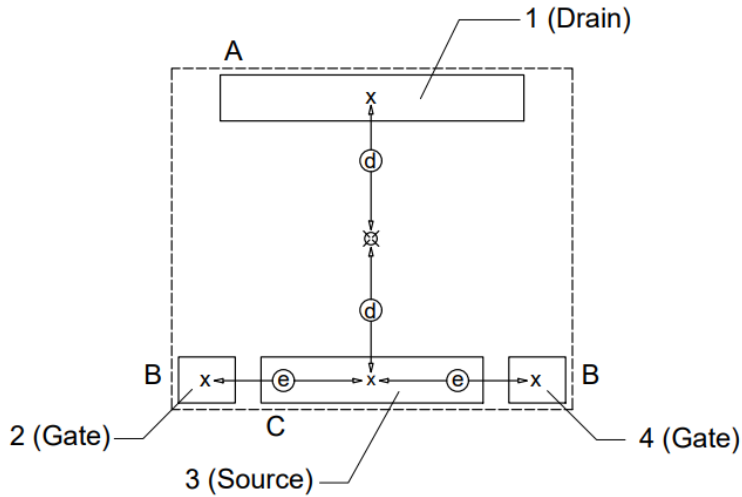
### Routing Guidelines

The following layout recommendations are highlighted. Additional detail is provided in Application Note at [www.gansystems.com](http://www.gansystems.com).



- ① Keep out area: Avoid placing traces or vias on the top layer of the PCB, directly underneath the package. This is to prevent potential electro-migration and solder mask isolation issues during high temperature or/and voltage operation.
- ② Symmetrical dual gates are provided for flexible layout and easy paralleling. Either gate drive can be used. If the second gate is not used, it should be left floating.
- ③ A separate Source Sense pin is not provided on our top-side products because of the ultra-low inductance of our GaN<sub>PMX</sub>® packaging. The Source Sense pin functionality can be implemented simply by routing a Kelvin connection at the side of the Source pad. This can be done at either side of the source pad for layout optimization.
- ④ Do not route vias within the Gate pad as it may affect long term solder joint reliability. For other pads, it is recommended to implement filled vias for better solder joint reliability.

### Recommended PCB Footprint





**Pad sizes**

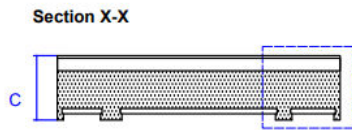
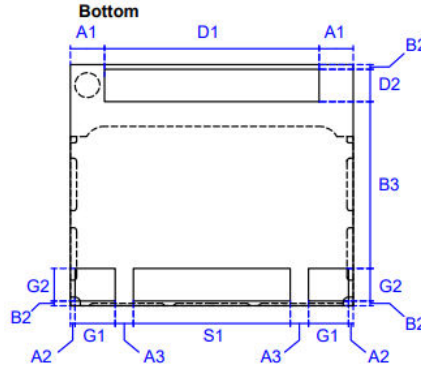
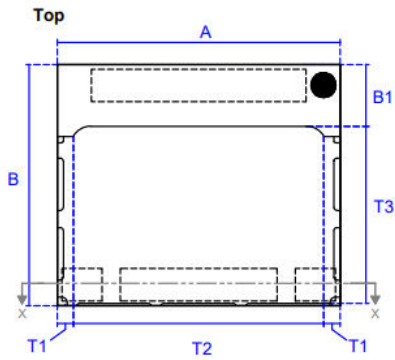
	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
<b>A</b>	6.94	1.05	0.273	0.041
<b>B</b>	1.30	1.05	0.051	0.041
<b>C</b>	5.07	1.05	0.200	0.041

**Dimensions**

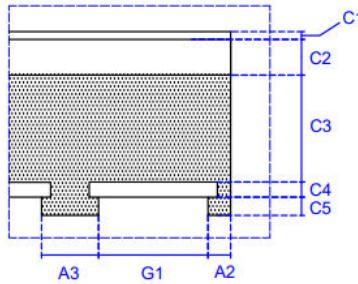
	mm	Inches
<b>d</b>	3.22	0.127
<b>e</b>	3.77	0.149

-  PCB pad openings
-  Package outline

### Package Dimensions



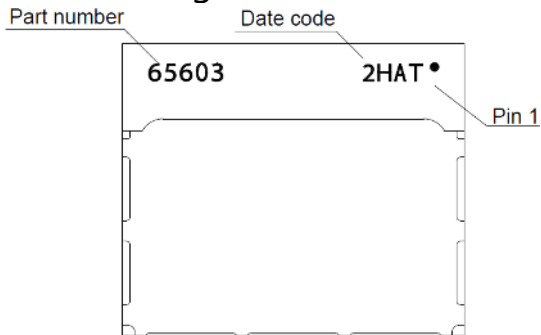
Surface Finish: ENIG  
Ni- 2.5um +/- 5um  
Au : 0.03 um +/-0.05um)



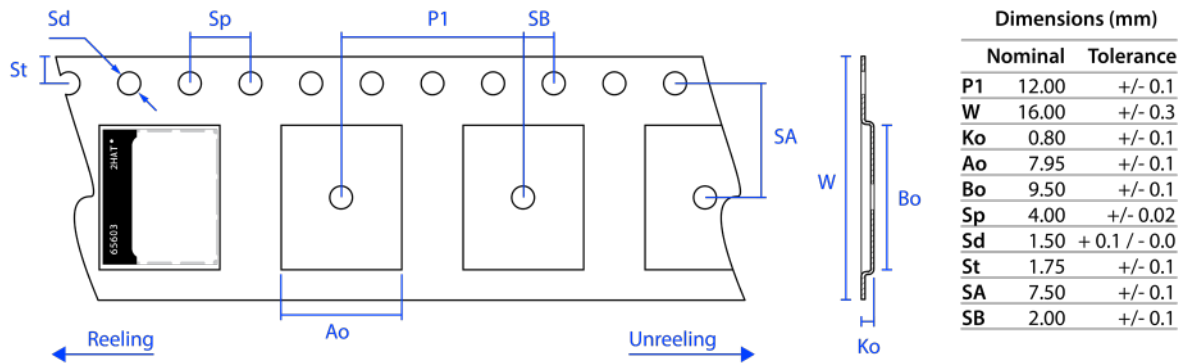
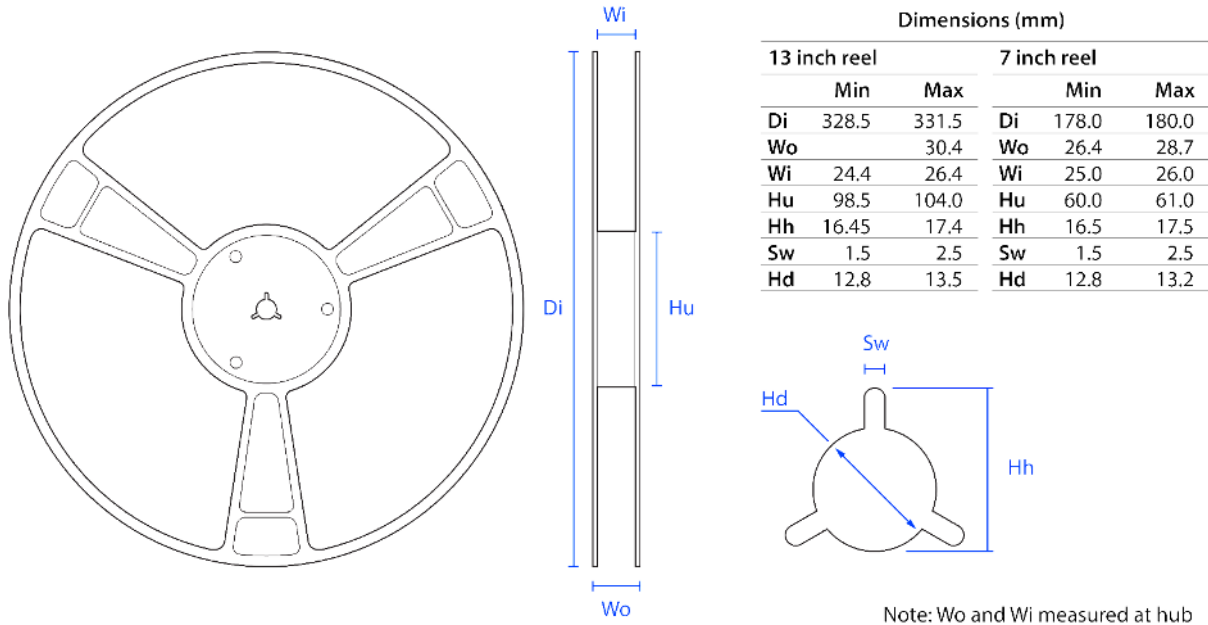
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A	9.15	0.360 +/- 0.100 mm (0.004")
A1	1.10	0.043 +/- 0.050 mm (0.002")
A2	0.15	0.006 +/- 0.050 mm (0.002")
A3	0.59	0.023
B	7.79	0.307 +/- 0.100 mm (0.004")
B1	2.00	0.079 +/- 0.050 mm (0.002")
B2	0.15	0.006 +/- 0.050 mm (0.002")
B3	5.39	0.212
C	0.49	0.019 +/- 0.072 mm (0.003")
C1	0.03	0.001
C2	0.11	0.004
C3	0.25	0.010
C4	0.04	0.002
C5	0.05	0.002
D1	6.94	0.273
D2	1.05	0.041
G1	1.30	0.051
G2	1.05	0.041
S1	5.07	0.200
T1	0.53	0.021
T2	8.09	0.319
T3	5.72	0.225

\*Inch measurements are approximate values

### Part Marking

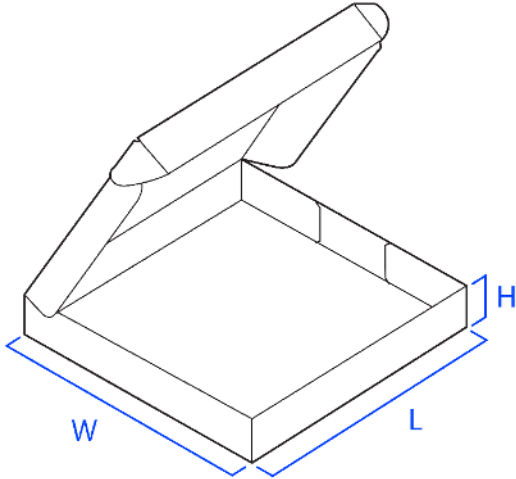


### Tape and Reel Information





## Tape and Reel Box Dimensions



**Outside dimensions (mm)**

		<b>13 inch reel</b>		<b>7 inch reel</b>	
		<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>
<b>W</b>		197.0	203.5	<b>W</b>	337.0 342.0
<b>L</b>		204.0	218.5	<b>L</b>	355.0
<b>H</b>			32.0	<b>H</b>	50.0 53.0

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