

H1M120F240

Silicon Carbide MOSFET
N-CHANNEL ENHANCEMENT MODE

Features

- Low On-Resistance and High Current Density
- Low Capacitance for High Frequency Operation
- Ultra-high Avalanche Ruggedness
- Positive Temperature Coefficient Device
- AEC-Q101 Qualified
- RoHS Compliant and Halogen Free

Benefits

- Higher System Efficiency
- Increase Parallel Device Convenience
- Capable of 175°C High T_j Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems

Applications

- Switching Mode Power Supply
- DC/DC Converters, UPS, and PFC
- EV Charging Station
- Motor Drives
- Power Inverters
- Solar/Wind Renewable Energy

Absolute Maximum Ratings (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Drain – Source Voltage	V _{DS,max}	V _{GS} =0V, I _{DS} =100μA	1200	V
Continuous Drain Current	I _D	V _{GS} =20V, T _C =25°C	13.5	A
		V _{GS} =20V, T _C =110°C	9.5	
Pulse Drain Current	I _{D,pulse}	t _{PW} limitation per Fig.15	23	
Avalanche energy, Single Pulse	E _{AS}	V _{DD} =100V, I _D =5A	312	mJ
Power Dissipation	P _D	T _C =25°C	105	W
Recommend Gate Source Voltage	V _{GS,op}	Static, recommended DC operating values	-5 to 20	V
Maximum Gate Source Voltage	V _{GS,max}	Transient operating limit (AC f > 1Hz, duty cycle < 1%)	-10 to 25	
Junction & Storage Temperature	T _j , T _{stg}		-55 to 175	°C
Soldering Temperature	T _L		260	
Mounting Torque	M _D	M3 or 6-32 screw	1.0	Nm

Thermal Resistance

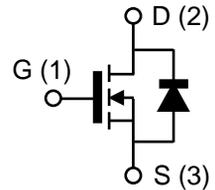
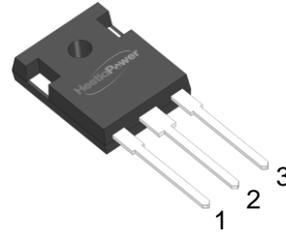
Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance, Junction to Case	R _{θ,jc}		1.42		°C/W

Product Summary

V _{DS}	1200V
I _D (@25°C)	13.5A
R _{DS(on)}	240mΩ



Circuit Diagram



Part Number	Package	Marking
H1M120F240	TO-247-3L	H1M120F240

Description

The H1M120F240 1200V, 240mΩ silicon carbide power MOSFET is an N-channel enhancement mode device. Exploiting the outstanding wide bandgap material properties, this device shows high current density and great switching behavior. Thanks for the excellent thermal conductivity and many advantages of SiC, this device significantly improved in thermal capability and temperature independent switching behavior. With the high stability and reliability, this device also passes the qualification criteria based on AEC-Q101.

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_{DS}=100\mu A$	1200			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=10V, I_{DS}=5mA$		2.6		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=1200V, V_{GS}=0V$		<1	50	μA
		$V_{DS}=1200V, V_{GS}=0V$ $T_j=175^\circ\text{C}$		10	500	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$			250	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=20V, I_{DS}=5A$		240	320	mΩ
		$V_{GS}=20V, I_{DS}=5A,$ $T_j=175^\circ\text{C}$		400		
Transconductance	g_{fs}	$V_{DS}=12V, I_{DS}=15A$		4.3		S
Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=800V$ $f=1MHz, V_{AC}=25mV$		559		pF
Output Capacitance	C_{oss}			36		
Reverse Transfer Capacitance	C_{rss}			7.5		
Effective Output Capacitance, Energy Related	$C_{o(er)}$	$V_{GS}=0V,$ $V_{DS}=0 \text{ to } 800V$		46		pF
Effective Output Capacitance, Time Related	$C_{o(tr)}$	$I_D=const., V_{GS}=0V,$ $V_{DS}=0 \text{ to } 800V$		62		
Turn On Delay Time	$t_{d(on)}$	$V_{DS}=800V, V_{GS}=0/20V,$ $I_D=4A, R_L=200\Omega,$ $R_{G(ext)}=10\Omega$		23		ns
Rise Time	t_r			19		
Turn Off Delay Time	$t_{d(off)}$			40		
Fall Time	t_f			64		
C_{oss} Stored Energy	E_{oss}	$V_{GS}=0V, V_{DS}=800V$ $f=1MHz, V_{AC}=25mV$		14		μJ
Turn-on Switching Energy	E_{on}	$V_{DS}=800V, V_{GS}=0/20V,$ $I_D=5A,$		10*		
Turn-off Switching Energy	E_{off}	$R_{G(ext)}=2.7\Omega$		10*		
Internal Gate Resistance	$R_{G(int.)}$	$f=1MHz, V_{AC}=25mV$		3.7		Ω

*Based on the results of calculation, note that the energy loss caused by the reverse recovery of free-wheeling diode is not included in E_{on} .

Built-in SiC Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ.	Unit
Inverse Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_{SD}=1.25A$	3.1	V
Continuous Diode Forward Current	I_S	$V_{GS}=0V, T_c=25^\circ\text{C}$	15.5	A
Reverse Recovery Time	t_{rr}	$V_{GS}=0V,$	47	ns
Reverse Recovery Charge	Q_{rr}	$I_{SD}=5A, V_{DS}=400V,$	36	nC
Peak Reverse Recovery Current	I_{rrm}	$di/dt=300A/\mu s$	1.5	A

Gate Charge Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Gate to Source Charge	Q_{GS}	$V_{DS}=800V,$ $V_{GS}=-5/+20V,$ $I_D=5A$	10	nC
Gate to Drain Charge	Q_{GD}		25	
Total Gate Charge	Q_G		47	
Gate plateau voltage	V_{pl}		8.5	V

Typical Device Performance

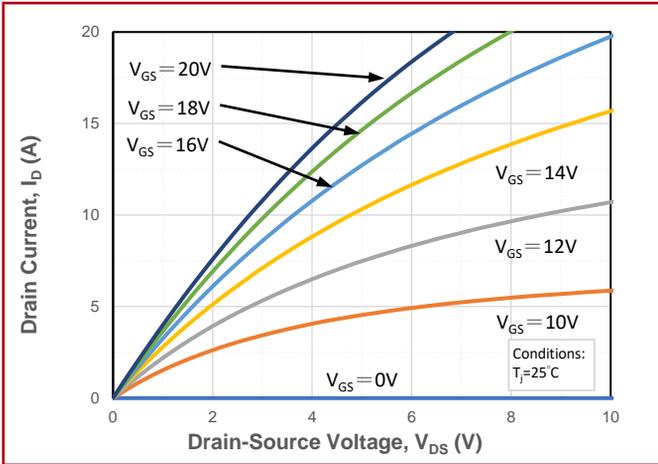


Fig.1 Forward Output Characteristics at $T_j = 25^\circ\text{C}$

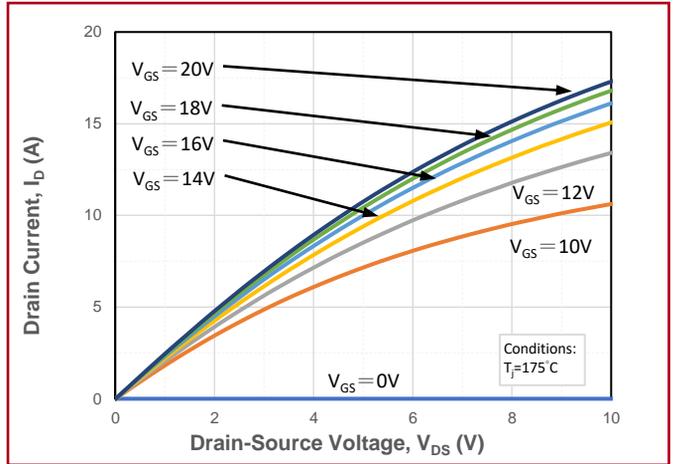


Fig.2 Forward Output Characteristics at $T_j = 175^\circ\text{C}$

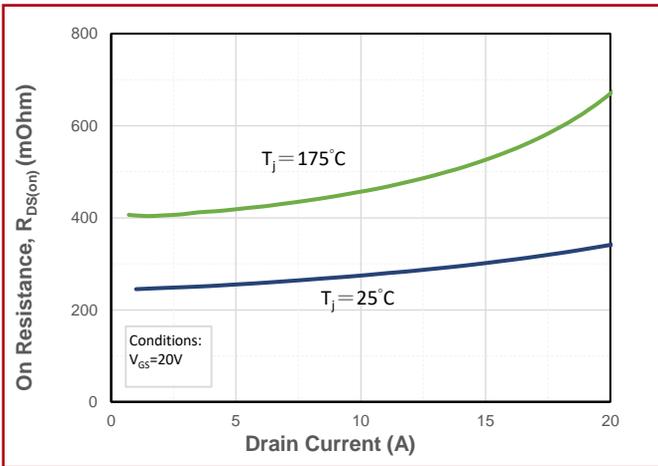


Fig.3 On-Resistance vs. Drain Current for Various T_j

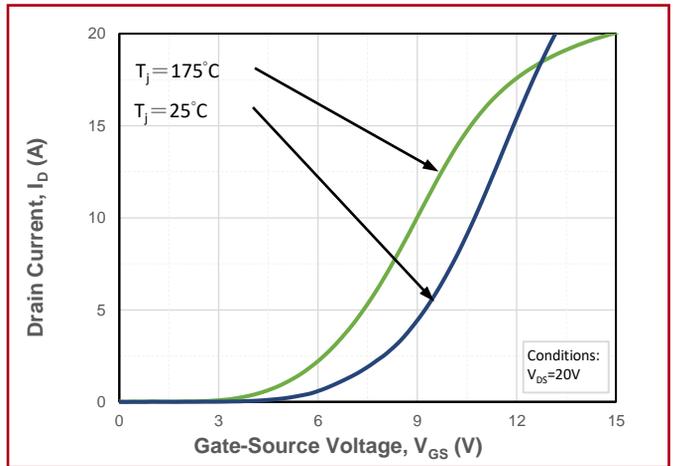


Fig.4 Transfer Characteristics for Various T_j

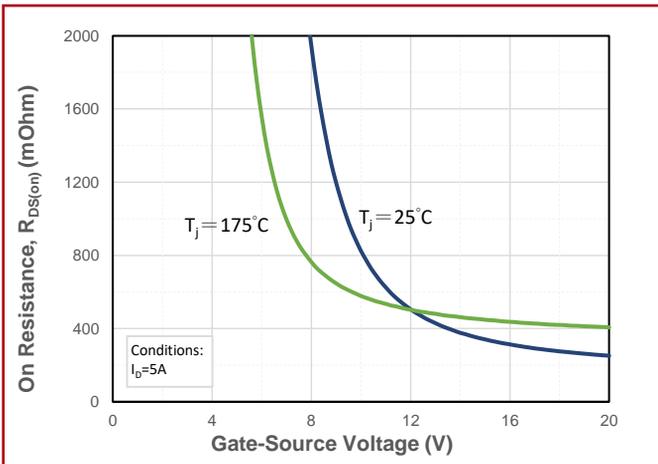


Fig.5 On-Resistance vs. Gate Voltage for Various T_j

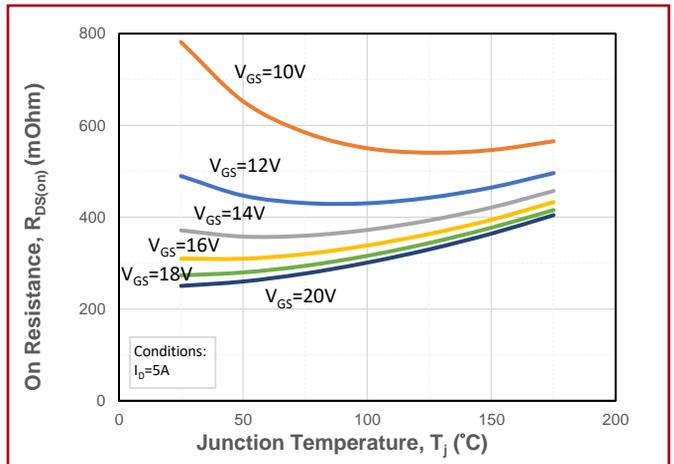


Fig.6 On-Resistance vs. Temperature for Various Gate Voltage

Typical Device Performance

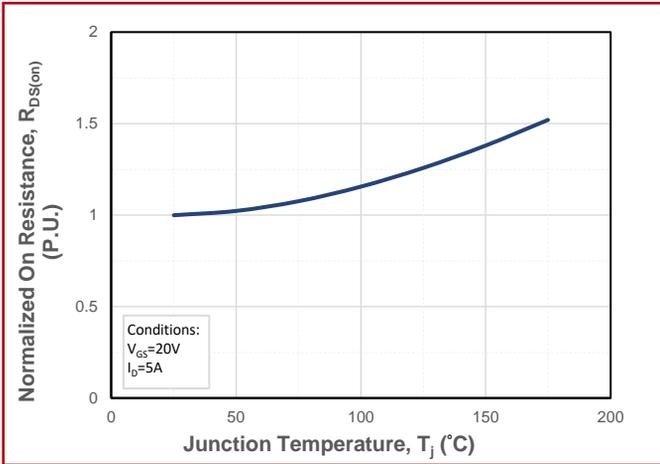


Fig.7 Normalized On-Resistance vs. Temperature

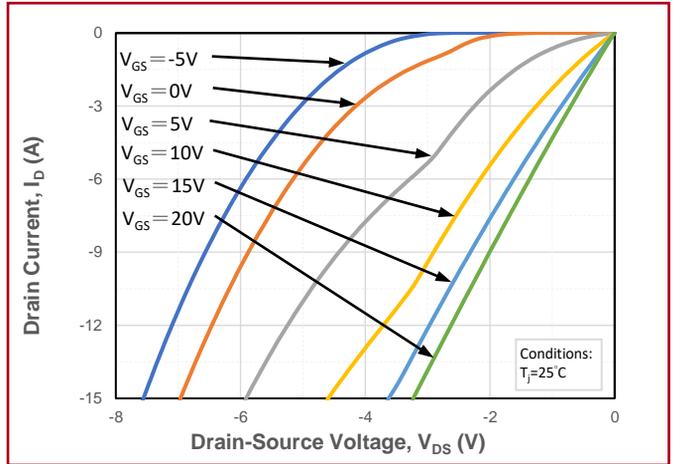


Fig.8 Reverse Output Characteristics at $T_j = 25^\circ C$

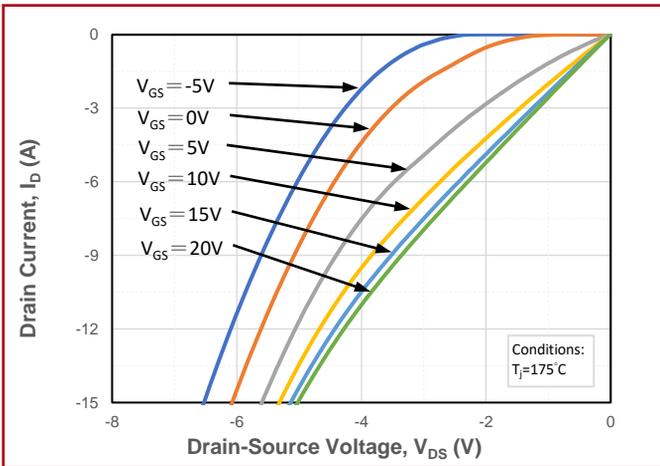


Fig.9 Reverse Output Characteristics at $T_j = 175^\circ C$

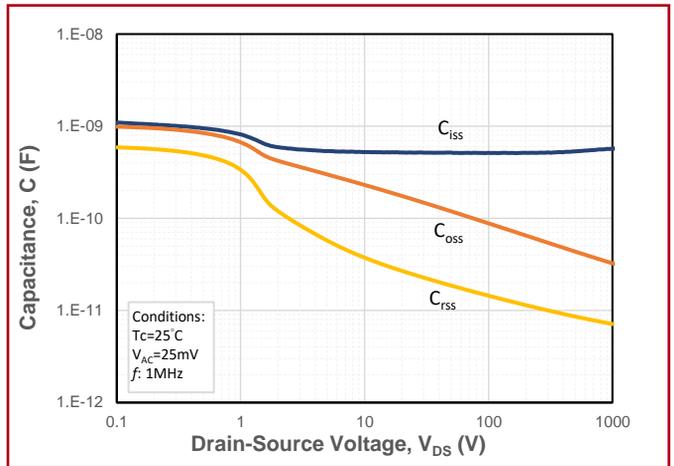


Fig.10 Capacitances vs. Drain to Source Voltage

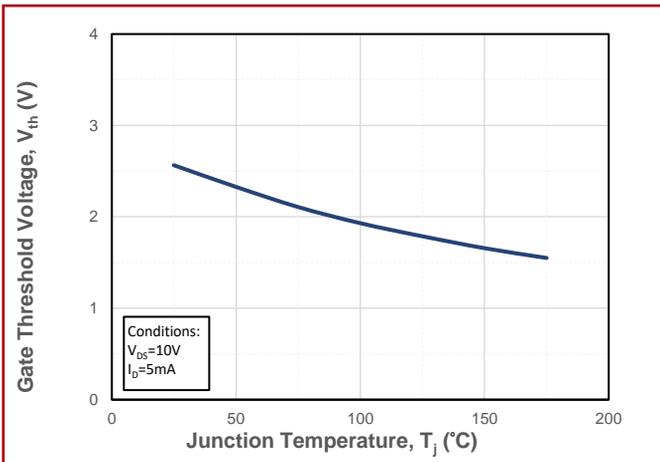


Fig.11 Threshold Voltage vs. Temperature

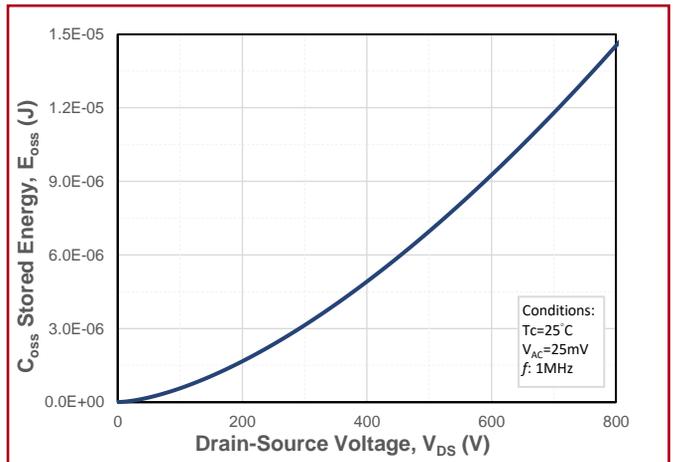


Fig.12 Output Capacitor Stored Energy

Typical Device Performance

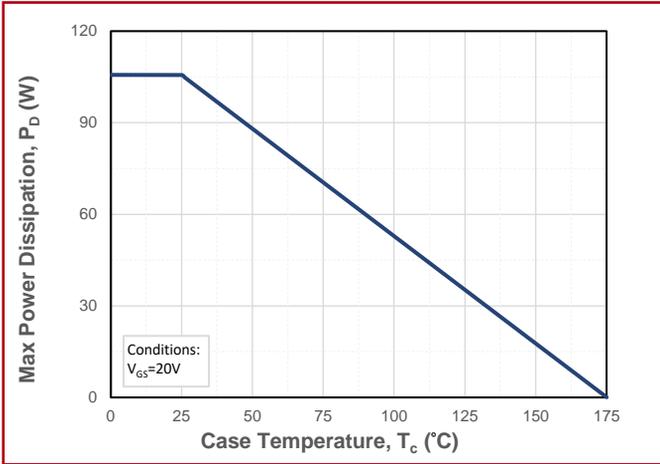


Fig.13 Maximum Power Dissipation Derating vs. Case Temperature

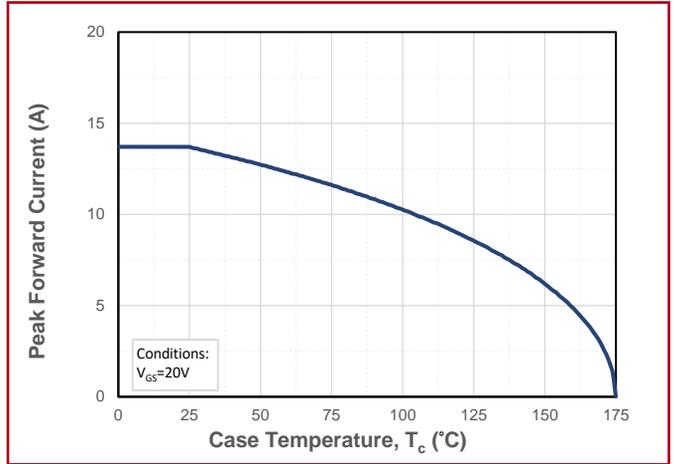


Fig.14 Drain Current Derating vs. Case Temperature

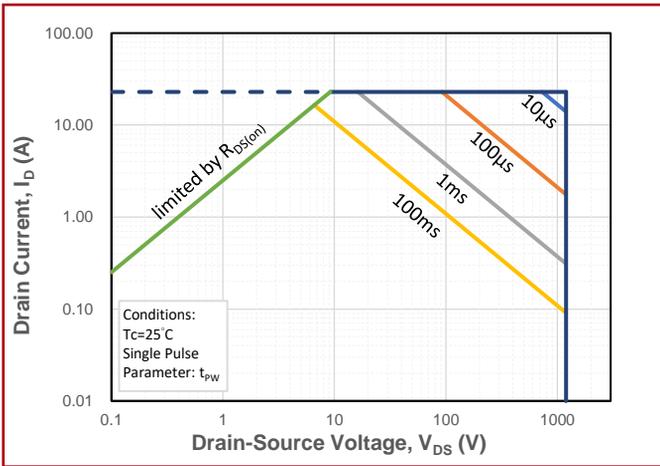


Fig.15 Safe Operating Area

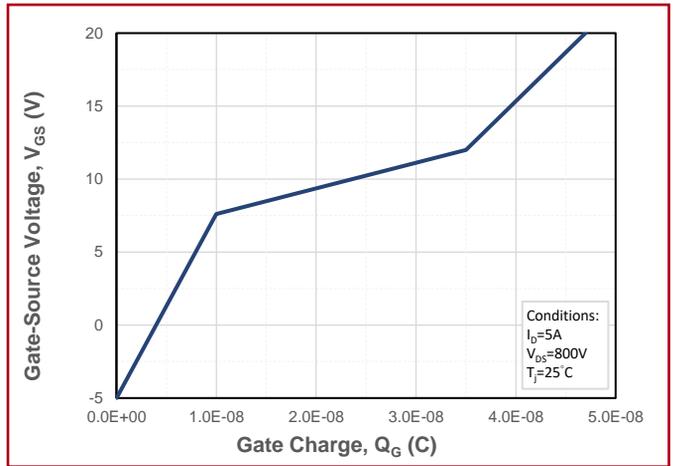


Fig.16 Gate Charge Characteristics

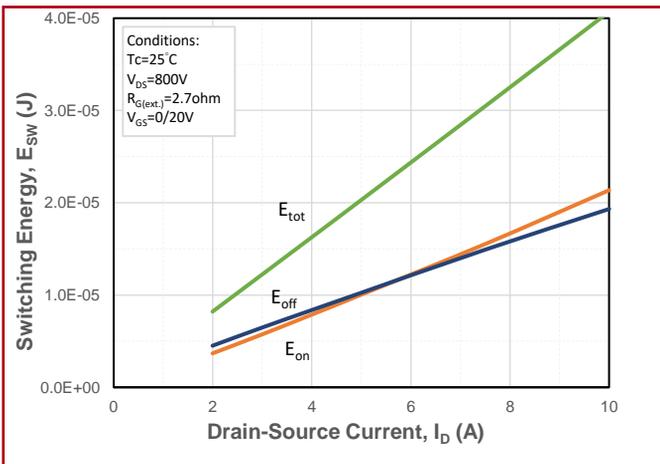


Fig.17 Clamped Inductive Switching Energy vs. Drain Current

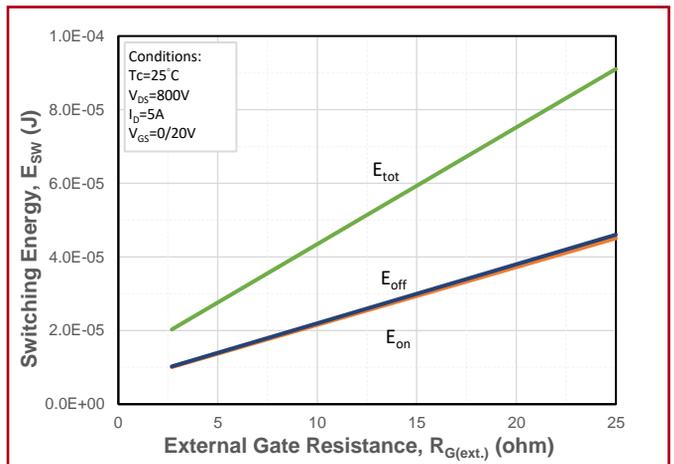


Fig.18 Clamped Inductive Switching Energy vs. External Gate Resistor (R_{G(ext.)})

Typical Device Performance

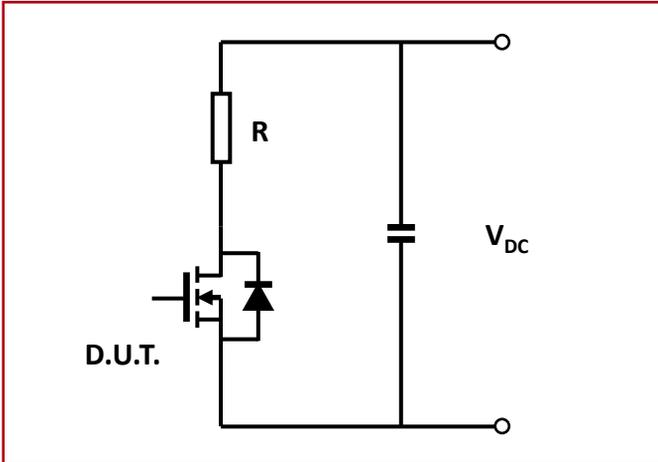


Fig.19 Schematic of Resistive Switching

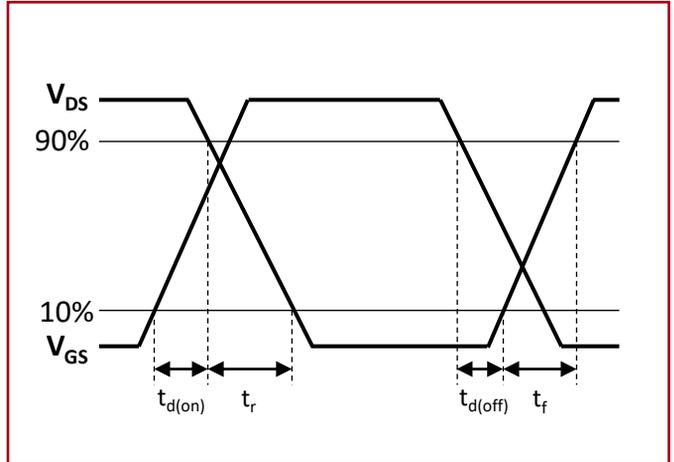


Fig.20 Switching Times Definition

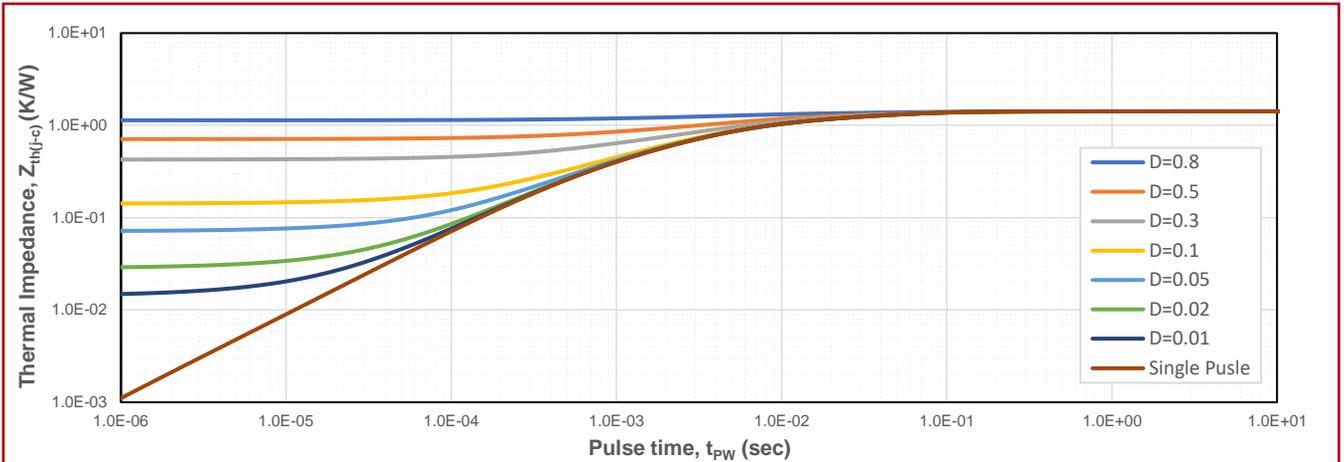


Fig.21 Transient Junction to Case Thermal Impedance

Naming Rule

H1 M 120 F 240

Generation

H1 = 1st Gen Discrete

Device Type

M = MOSFET J = JMOS

S = JBS diode

Breakdown Voltage

065 = 650V 170 = 1700V

120 = 1200V 330 = 3300V

Package

F = TO-247-3L B = TO-220-3L

T = TO-263-2L N = Bare Die

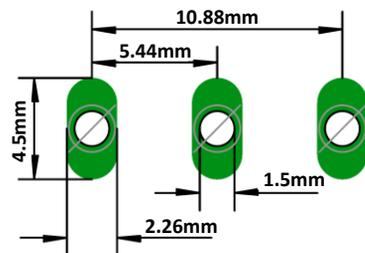
Typical On-Resistance

030 = 30mΩ 060 = 60mΩ 120 = 120mΩ

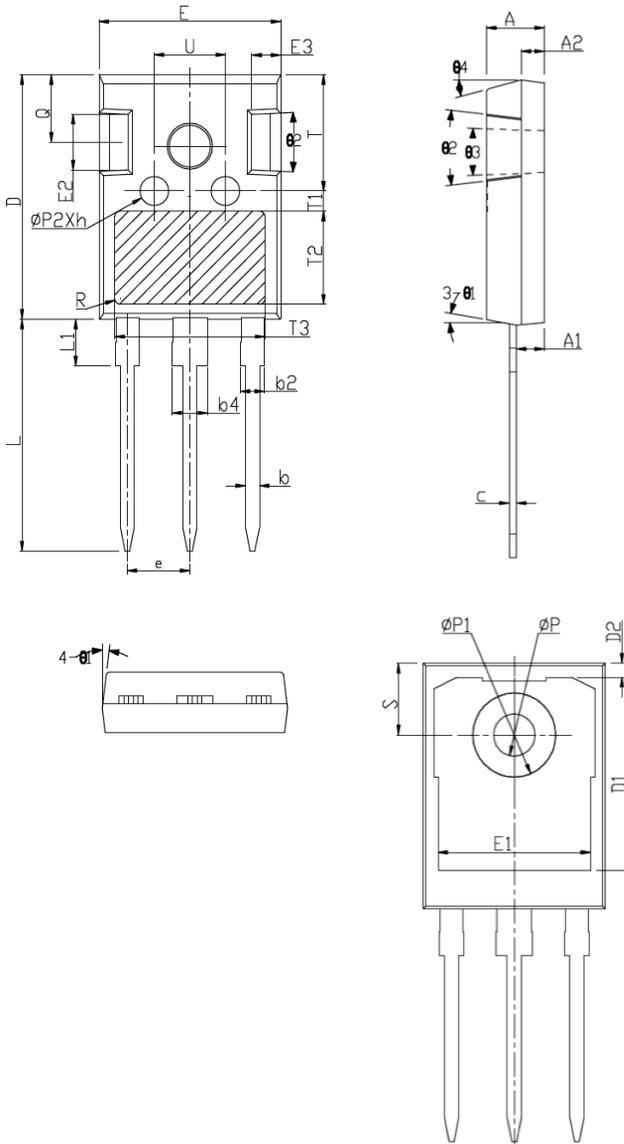
240 = 240mΩ

Recommended Solder Pad Layout

TO-247-3L



Package Dimensions



Symbol	mm		
	Min.	Typ.	Max.
A	4.75	5.00	5.25
A1	2.16	2.41	2.66
A2	1.85	2.00	2.15
b	1.11	1.21	1.35
b2	1.90	2.01	2.25
b4	2.90	3.01	3.25
c	0.51	0.61	0.75
D	20.60	21.00	21.40
D1	16.15	16.55	16.95
D2	1.00	1.20	1.40
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.70	5.00	5.30
E3	2.25	2.50	2.75
e	5.44 BSC		
h	0.00	0.10	0.25
L	19.52	19.92	20.32
L1	-	-	4.30
ØP	3.35	3.60	3.85
ØP1	-	-	7.30
ØP2	2.25	2.50	2.75
Q	5.50	5.80	6.10
S	6.15 BSC		
R	0.50 REF		
T	9.70	-	10.30
T1	1.65 REF		
T2	8.00 REF		
T3	12.80 REF		
U	5.90	-	6.50
Ø1	4°	7°	10°
Ø2	2°	5°	8°
Ø3	1°	-	2°
Ø4	10°	15°	20°

Notes

- The information provided herein is subject to change without notice.
- For other information that does not show on this datasheet, please contact us for inquiry.