H1M065F200

Silicon Carbide MOSFET
N-CHANNEL ENHANCEMENT MODE

Features

- Low On-Resistance and High Current Density
- Low Capacitance for High Frequency Operation
- Ultra-high Avalanche Ruggedness
- Positive Temperature Coefficient Device
- AEC-Q101 Qualified
- RoHS Compliant and Halogen Free

Benefits

- Higher System Efficiency
- Increase Parallel Device Convenience
- Capable of 175˚C High T_j Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems

Applications

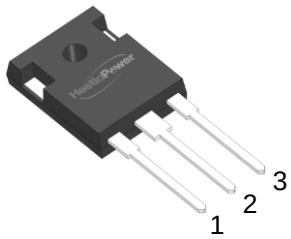
- Switching Mode Power Supply
- DC/DC Converters, UPS, and PFC
- EV Charging Station
- Motor Drives
- Power Inverters
- Solar/Wind Renewable Energy

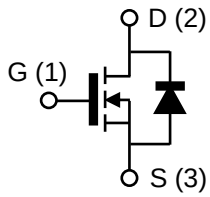
Product Summary

V_{DS}	650V
$I_{D(@25˚C)}$	18.5A
$R_{DS(on)}$	200mΩ

RoHS COMPLIANT
Halogen-Free F Cl I Br
AEC-Q101 QUALIFIED

Circuit Diagram





Part Number	Package	Marking
H1M065F200	TO-247-3L	H1M065F200

Description

The H1M065F200 650V, 200mΩ silicon carbide power MOSFET is an N-channel enhancement mode device. Exploiting the outstanding wide bandgap material properties, this device shows high current density and great switching behavior. Thanks for the excellent thermal conductivity and many advantages of SiC, this device significantly improved in thermal capability and temperature independent switching behavior. With the high stability and reliability, this device also passes the qualification criteria based on AEC-Q101.

Absolute Maximum Ratings (T_c = 25˚C unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Drain – Source Voltage	$V_{DS, max}$	V_{GS}=0V, I_{DS}=100μA	650	V
Continuous Drain Current	I_D	V_{GS}=20V, T_C=25°C	18.5	A
		V_{GS}=20V, T_C=110°C	12.5	
Pulse Drain Current	$I_{D, pulse}$	t_{PW} limitation per Fig.15	34.5	
Avalanche energy, Single Pulse	E_{AS}	V_{DD}=100V, I_D=5A	400	mJ
Power Dissipation	P_D	T_C=25°C	105	W
Recommend Gate Source Voltage	$V_{GS, op}$	Static, recommended DC operating values	-5 to 20	V
Maximum Gate Source Voltage	$V_{GS, max}$	Transient operating limit (AC f > 1Hz, duty cycle < 1%)	-10 to 25	
Junction & Storage Temperature	T_j, T_{stg}		-55 to 175	°C
Soldering Temperature	T_L		260	
Mounting Torque	M_D	M3 or 6-32 screw	1.0	Nm

Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance, Junction to Case	$R_{θ,JC}$		1.42		˚C/W

Electrical Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_{DS}=100μA	650			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=10V, I_{DS}=5mA		2.6		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V		<1	50	μA
		V_{DS}=650V, V_{GS}=0V T_j=175°C		5	500	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=20V, V_{DS}=0V			250	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=20V, I_{DS}=6A		200	260	mΩ
		V_{GS}=20V, I_{DS}=6A, T_j=175°C		260		
Transconductance	g_{fs}	V_{DS}=17V, I_{DS}=15A		4.5		S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=400V f =1MHz, V_{AC}=25mV		498		pF
Output Capacitance	C_{oss}			59		
Reverse Transfer Capacitance	C_{rss}			8		
Effective Output Capacitance, Energy Related	$C_{o(er)}$	V_{GS}=0V, V_{DS}=0 to 400V		74.5		
Effective Output Capacitance, Time Related	$C_{o(tr)}$	I_D=const., V_{GS}=0V, V_{DS}=0 to 400V		100		
Short-Circuit Withstand Time	t_{SC}	V_{GS}=0/15V, V_{DS}=400V R_G=100Ω		<18		μs
Turn On Delay Time	$t_{d(on)}$	V_{DS}=400V, V_{GS}=-4/+20V, I_D=5A, R_L=80Ω, $R_{G(ext)}$= 2.7 Ω		15		ns
Rise Time	t_r			17		
Turn Off Delay Time	$t_{d(off)}$			17		
Fall Time	t_f			20		
C_{oss} Stored Energy	E_{oss}	V_{GS}=0V, V_{DS}=400V f =1MHz, V_{AC}=25mV		5.7		μJ
Turn-on Switching Energy	E_{on}	V_{DS}=400V, V_{GS}=0/20V, I_D=6A, $R_{G(ext)}$= 2.7 Ω		2.9*		
Turn-off Switching Energy	E_{off}			3.8*		
Internal Gate Resistance	$R_{G(int.)}$	f =1MHz, V_{AC}=25mV		3.6		Ω

*Based on the results of calculation, note that the energy loss caused by the reverse recovery of free-wheeling diode is not included in E_{on}.

Built-in SiC Diode Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ.	Unit
Inverse Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_{SD}=2A	3.5	V
Continuous Diode Forward Current	I_S	V_{GS}=0V, T_C=25°C	16	A
Reverse Recovery Time	t_{rr}	V_{GS}=0V, I_{SD}=5A, V_{DS}=400V, di/dt=300A/μs	50	ns
Reverse Recovery Charge	Q_{rr}		35	nC
Peak Reverse Recovery Current	I_{rrm}		1.8	A

Gate Charge Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Gate to Source Charge	Q_{GS}	V_{DS}=400V, V_{GS}=-5/+20V, I_D=5A	10	nC
Gate to Drain Charge	Q_{GD}		19	
Total Gate Charge	Q_G		43	
Gate plateau voltage	V_{pl}		8.7	V

Typical Device Performance

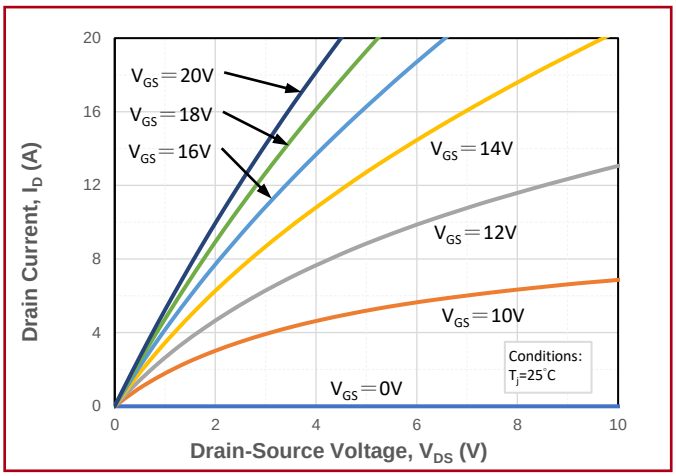


Fig.1 Forward Output Characteristics at T_j=25˚C

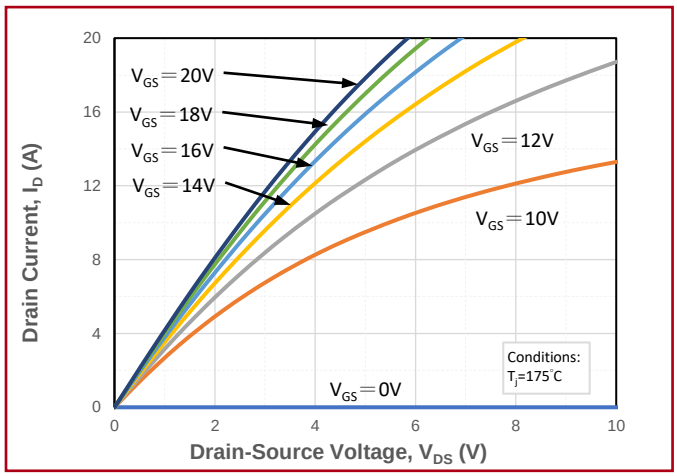


Fig.2 Forward Output Characteristics at T_j=175˚C

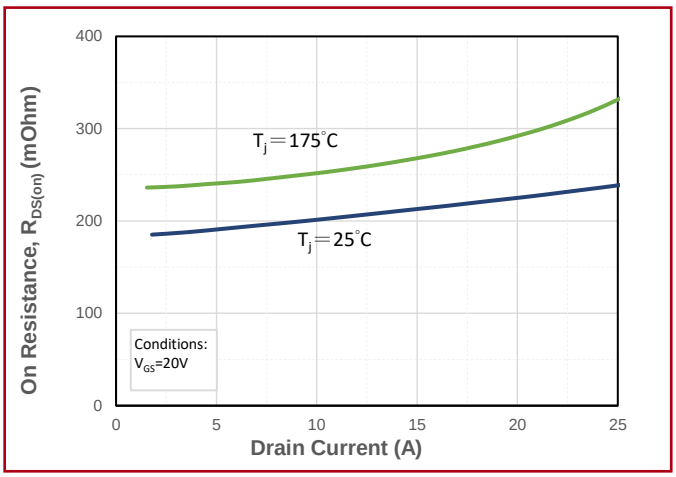


Fig.3 On-Resistance vs. Drain Current for Various T_j

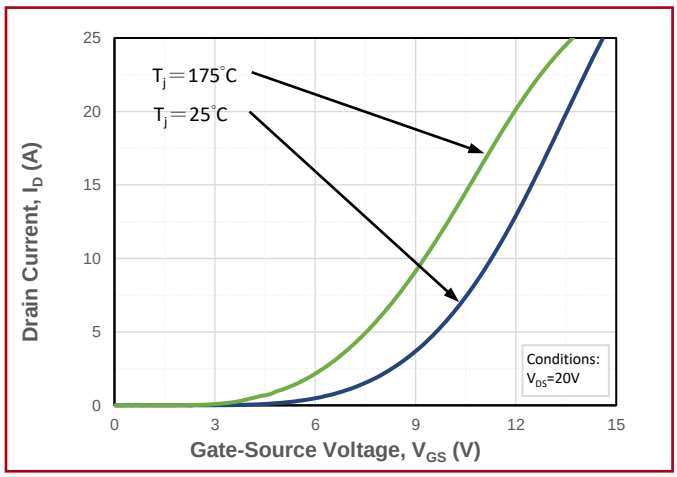


Fig.4 Transfer Characteristics for Various T_j

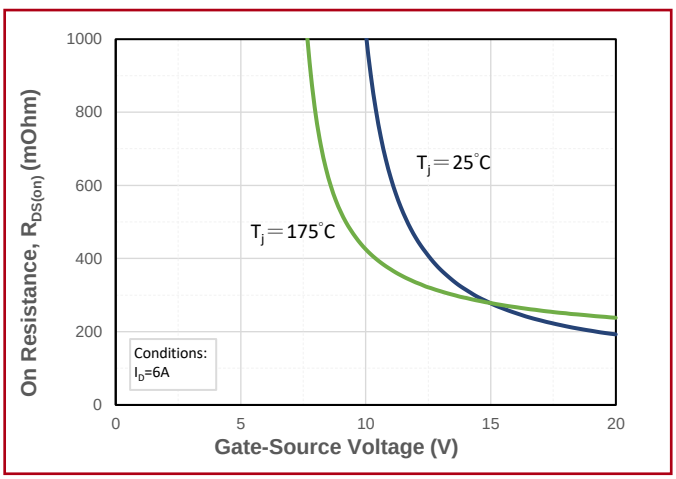


Fig.5 On-Resistance vs. Gate Voltage for Various T_j

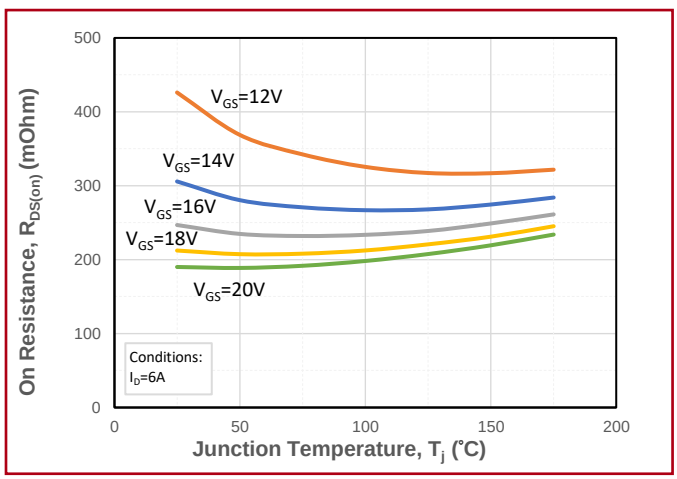


Fig.6 On-Resistance vs. Temperature for Various Gate Voltage

Typical Device Performance

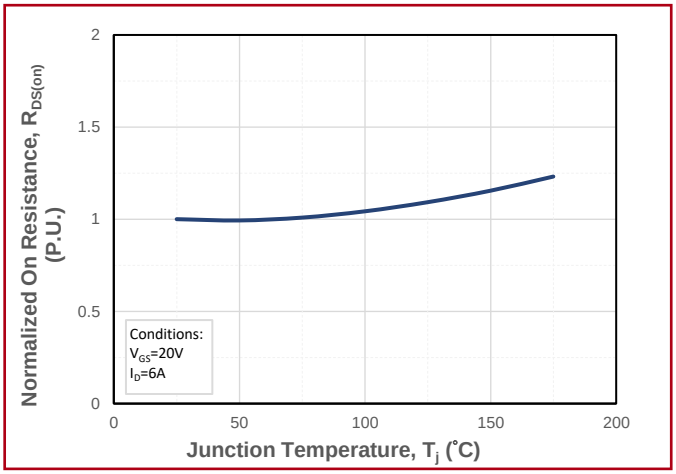


Fig.7 Normalized On-Resistance vs. Temperature

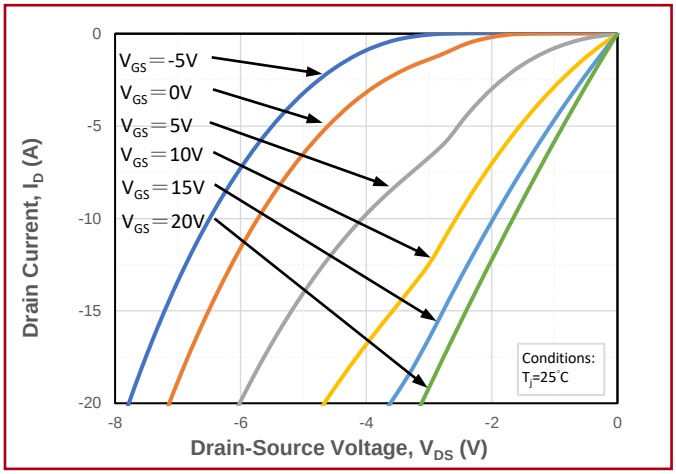


Fig.8 Reverse Output Characteristics at T_j = 25°C

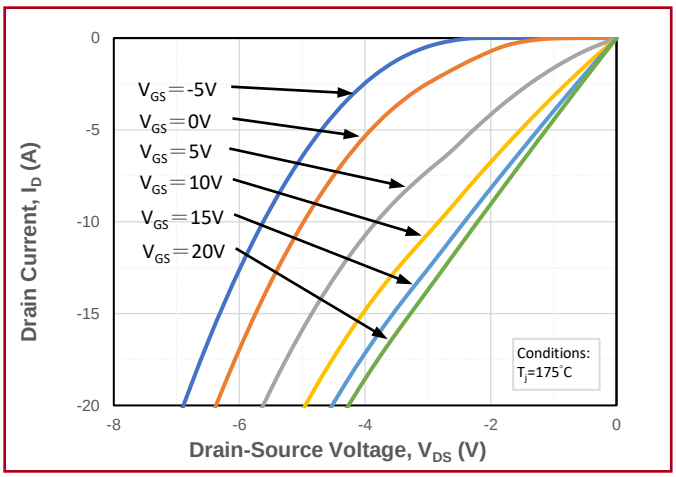


Fig.9 Reverse Output Characteristics at T_j = 175°C

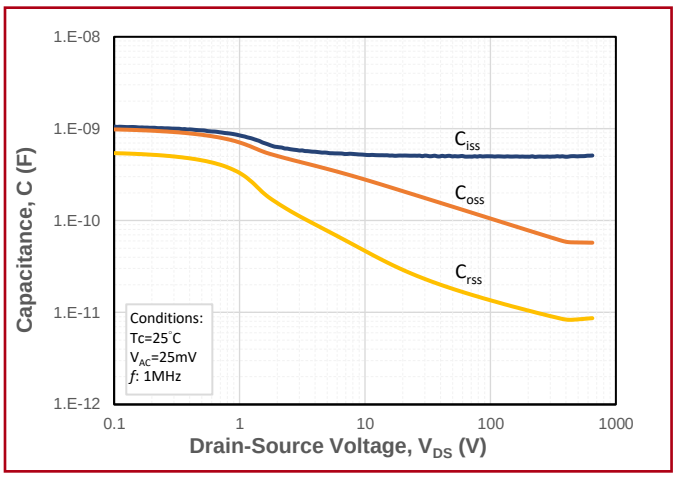


Fig.10 Capacitances vs. Drain to Source Voltage

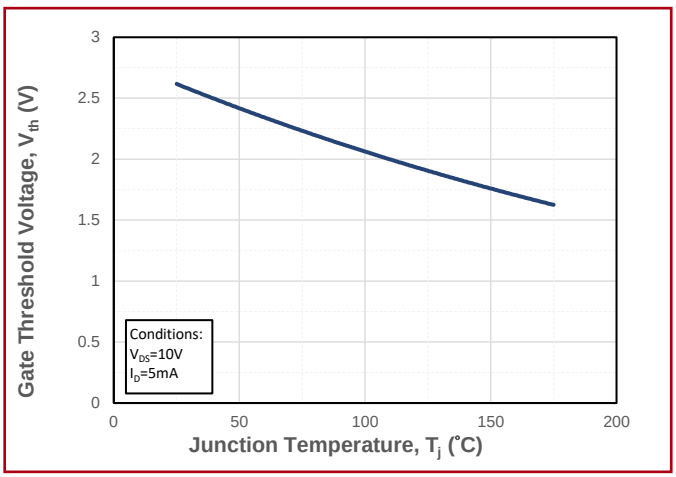


Fig.11 Threshold Voltage vs. Temperature

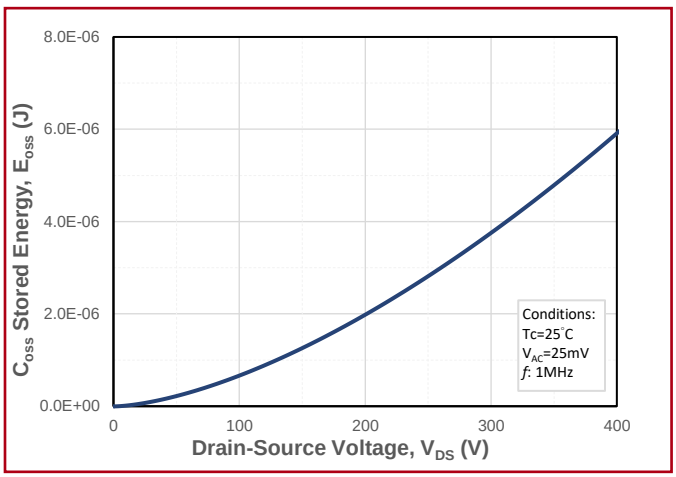


Fig.12 Output Capacitor Stored Energy

Typical Device Performance

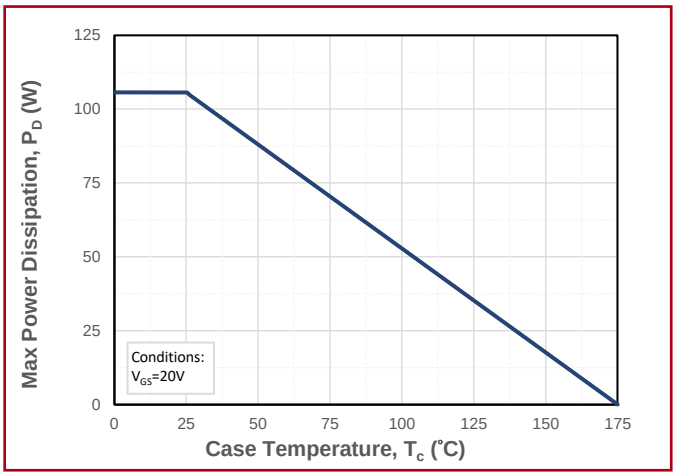


Fig.13 Maximum Power Dissipation Derating vs. Case Temperature

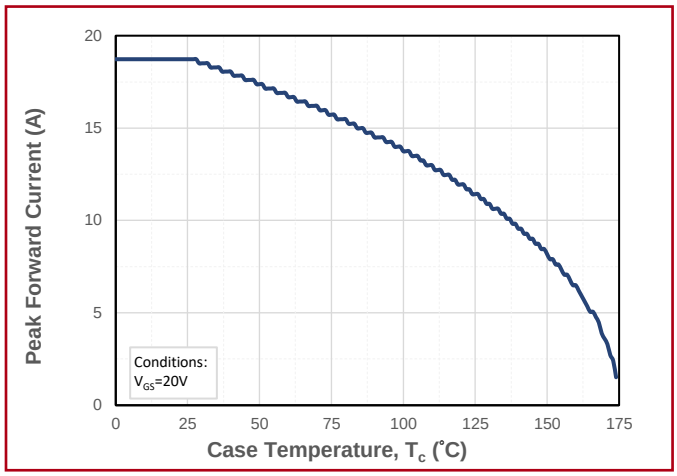


Fig.14 Drain Current Derating vs. Case Temperature

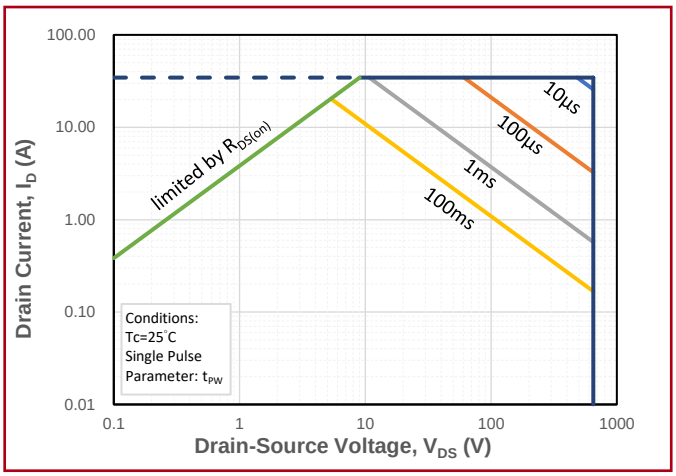


Fig.15 Safe Operating Area

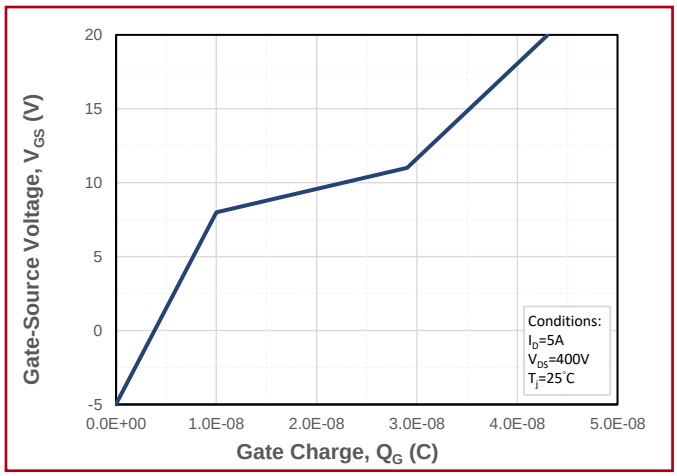


Fig.16 Gate Charge Characteristics

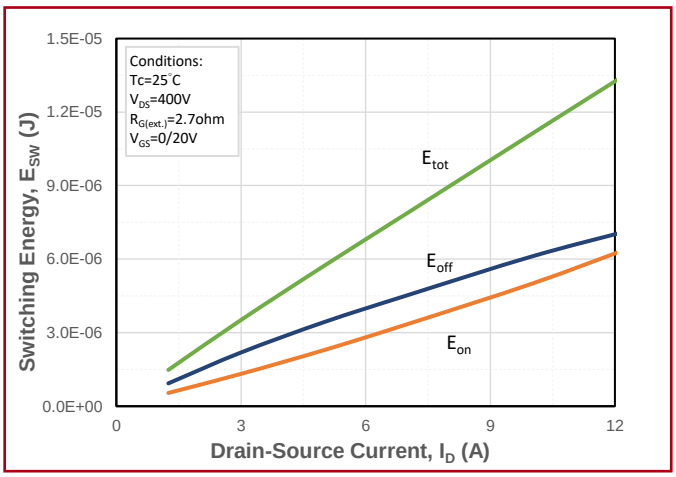


Fig.17 Clamped Inductive Switching Energy vs. Drain Current

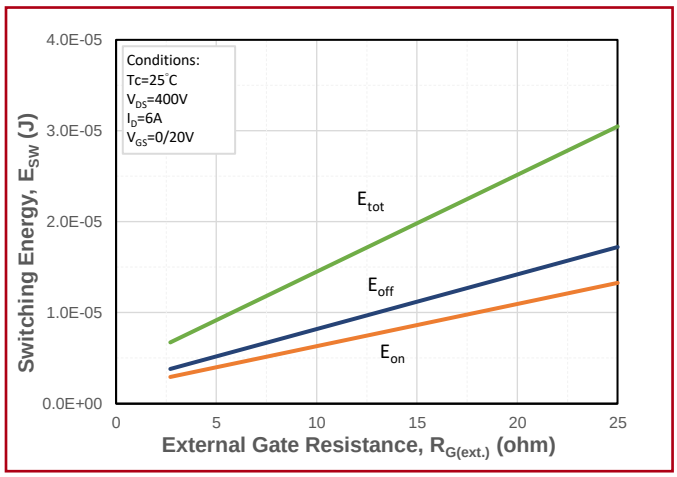


Fig.18 Clamped Inductive Switching Energy vs. External Gate Resistor ($R_{G(ext.)}$)

Typical Device Performance

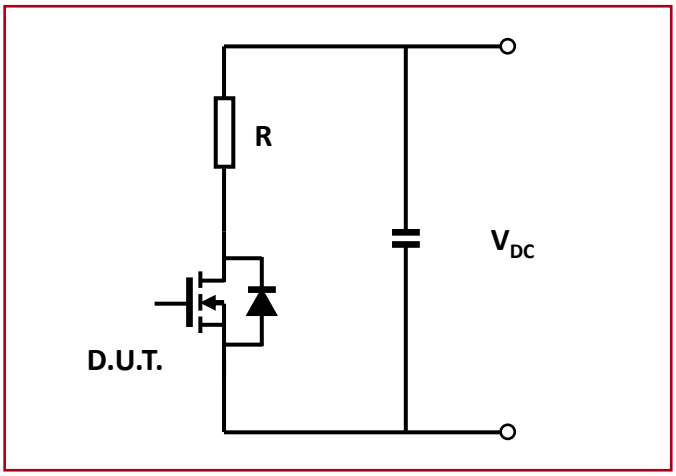


Fig.19 Schematic of Resistive Switching

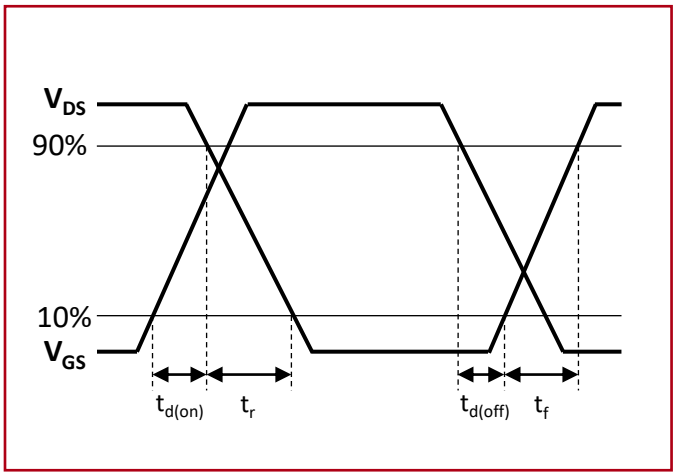


Fig.20 Switching Times Definition

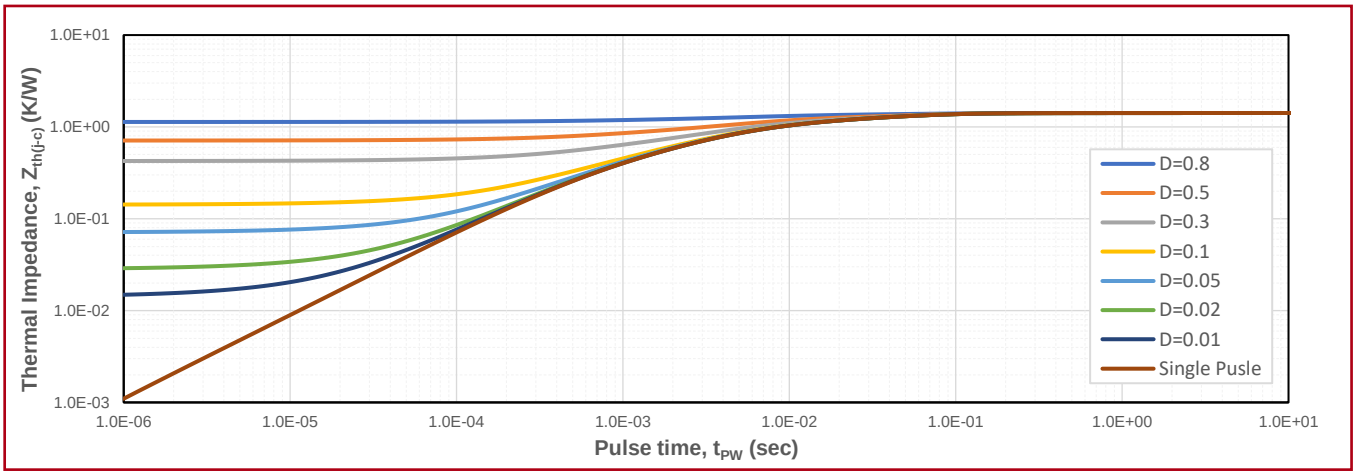


Fig.21 Transient Junction to Case Thermal Impedance

Naming Rule

H1 M 065 F 200

Generation
H1 = Gen 1st Discrete

Device Type
M = MOSFET J = JMOS
S = JBS diode

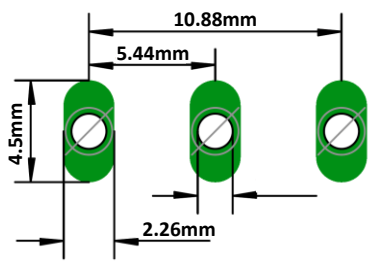
Breakdown Voltage
065 = 650V 170 = 1700V
120 = 1200V 330 = 3300V

Package
F = TO-247-3L B = TO-220-3L
T = TO-263-2L N = Bare Die

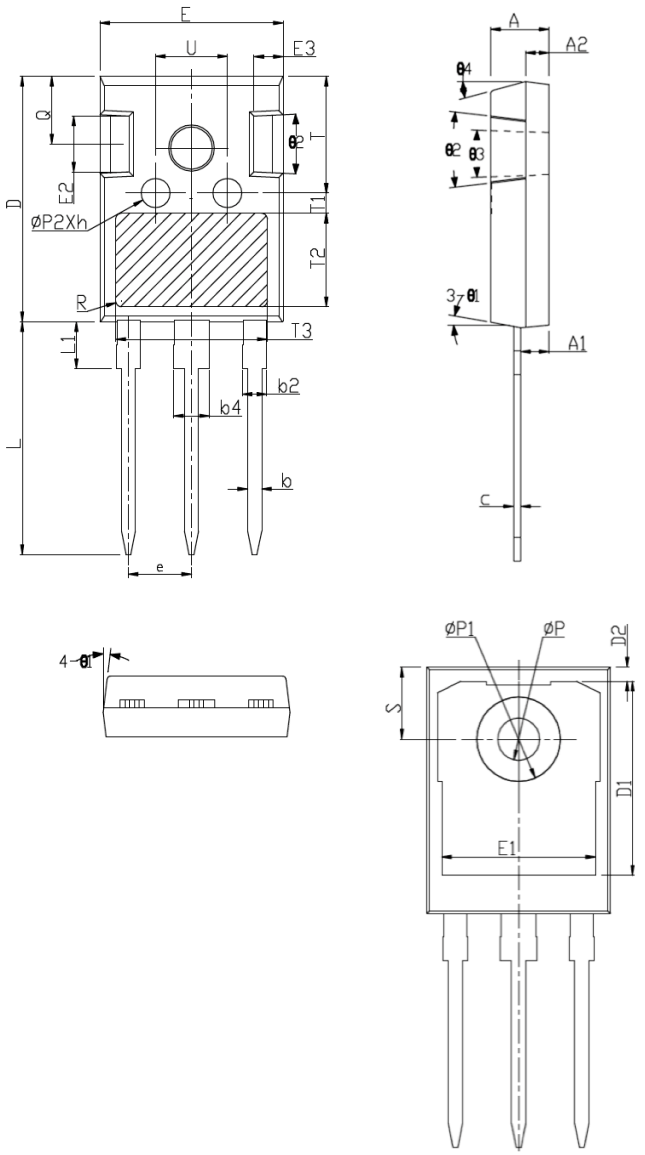
Typical On-Resistance
020 = 20mΩ 050 = 50mΩ 100 = 100mΩ
200 = 200mΩ

Recommended Solder Pad Layout

TO-247-3L



Package Dimensions



Symbol	mm		
	Min.	Typ.	Max.
A	4.75	5.00	5.25
A1	2.16	2.41	2.66
A2	1.85	2.00	2.15
b	1.11	1.21	1.35
b2	1.90	2.01	2.25
b4	2.90	3.01	3.25
c	0.51	0.61	0.75
D	20.60	21.00	21.40
D1	16.15	16.55	16.95
D2	1.00	1.20	1.40
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.70	5.00	5.30
E3	2.25	2.50	2.75
e		5.44 BSC	
h	0.00	0.10	0.25
L	19.52	19.92	20.32
L1	-	-	4.30
ϕP	3.35	3.60	3.85
ϕP1	-	-	7.30
ϕP2	2.25	2.50	2.75
Q	5.50	5.80	6.10
S		6.15 BSC	
R		0.50 REF	
T	9.70	-	10.30
T1		1.65 REF	
T2		8.00 REF	
T3		12.80 REF	
U	5.90	-	6.50
θ1	4°	7°	10°
θ2	2°	5°	8°
θ3	1°	-	2°
θ4	10°	15°	20°

Notes

- The information provided herein is subject to change without notice.
- For other information that does not show on this datasheet, please contact us for inquiry.