

# H1M065B200

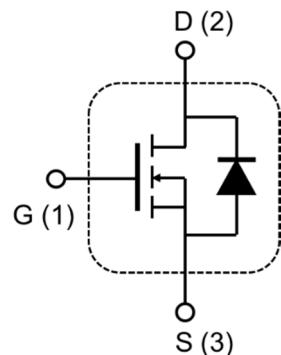
Silicon Carbide Power MOSFET

N-CHANNEL ENHANCEMENT MODE

TO-220-3L



Inner Circuit



## Product Summary

$V_{DS}$	650V
$I_D(@25^\circ C)$	16A
$R_{DS(on)}$	200mΩ



## Features

- ◆ Low On-Resistance
- ◆ Low Capacitance
- ◆ Avalanche Ruggedness
- ◆ Halogen Free, RoHS Compliant

## Applications

- ◆ SMPS / UPS / PFC
- ◆ EV Charging station & Motor Drives
- ◆ Power Inverters & DC/DC Converters
- ◆ Solar/ Wind Renewable Energy

## Benefits

- ◆ Higher System Efficiency
- ◆ Parallel Device Convenience
- ◆ High Temperature Application
- ◆ High Frequency Operation

## Maximum Ratings ( $T_c=25^\circ C$ )

Parameter	Symbol	Test Conditions	Value	Unit
Drain – Source Voltage	$V_{DS, max}$	$V_{GS}=0V, I_{DS}=100\mu A$	650	V
Continuous Drain Current	$I_D$	$V_{GS}=20V, T_c=25^\circ C$	16	A
		$V_{GS}=20V, T_c=110^\circ C$	10	
Pulse Drain Current	$I_{D, pulse}$	$t_{PW}$ limitation per Fig.16	28	
Avalanche energy, Single Pulse	$E_{AS}$	$V_{DD}=100V, I_D=5A$	312	mJ
Power Dissipation	$P_D$	$T_c=25^\circ C$	89	W
Recommend Gate Source Voltage	$V_{GS, op}$		-5/+20	V
Maximum Gate Source Voltage	$V_{GS, max}$		-10/+25	
Junction & Storage Temperature	$T_j, T_{stg}$		-55/+150	°C
Soldering Temperature	$T_L$		260	

## Electrical Characteristics ( $T_j=25^\circ\text{C}$ )

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{DS}}=100\mu\text{A}$	650			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=10\text{V}, I_{\text{DS}}=2.5\text{mA}$		2.2		V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}}=650\text{V}, V_{\text{GS}}=0\text{V}$		<1	50	$\mu\text{A}$
		$V_{\text{DS}}=650\text{V}, V_{\text{GS}}=0\text{V}$ $T_j=150^\circ\text{C}$		5	200	
Gate-Source Leakage Current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{V}, V_{\text{DS}}=0\text{V}$			250	nA
Drain-Source On-State Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=20\text{V}, I_{\text{DS}}=5\text{A}$	200	260		$\text{m}\Omega$
		$V_{\text{GS}}=20\text{V}, I_{\text{DS}}=5\text{A},$ $T_j=150^\circ\text{C}$		270		
Input Capacitance	$C_{\text{iss}}$	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=400\text{V}$ $f=1\text{MHz}, V_{\text{AC}}=25\text{mV}$		515		$\text{pF}$
Output Capacitance	$C_{\text{oss}}$			67		
Reverse Transfer Capacitance	$C_{\text{rss}}$			16		
Effective Output Capacitance, Energy Related	$C_{\text{o(er)}}$	$V_{\text{GS}}=0\text{V},$ $V_{\text{DS}}=0 \text{ to } 400\text{V}$		72		
Effective Output Capacitance, Time Related	$C_{\text{o(tr)}}$	$I_D=\text{const.}, V_{\text{GS}}=0\text{V},$ $V_{\text{DS}}=0 \text{ to } 400\text{V}$		88		
Turn On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DS}}=400\text{V}, V_{\text{GS}}=-$ $4/+20\text{V}, I_D=5\text{A},$ $R_L=80\Omega,$ $R_{\text{G(ext)}}= 2.7 \Omega$		15		$\text{ns}$
Rise Time	$t_r$			17		
Turn Off Delay Time	$t_{\text{d(off)}}$			17		
Fall Time	$t_f$			20		
$C_{\text{oss}}$ Stored Energy	$E_{\text{oss}}$	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=400\text{V}$ $f=1\text{MHz}, V_{\text{AC}}=25\text{mV}$		7*		$\mu\text{J}$
Turn-on Switching Energy	$E_{\text{on}}$	$V_{\text{DS}}=400\text{V},$ $V_{\text{GS}}=0/20\text{V}, I_D=5\text{A},$ $R_{\text{G(ext)}}= 2.7 \Omega$		4*		
Turn-off Switching Energy	$E_{\text{off}}$			5*		
Internal Gate Resistance	$R_{\text{G(int.)}}$	$f=1\text{MHz}, V_{\text{AC}}=25\text{mV}$		3.6		$\Omega$

\*Base on the results of calculation, note that the energy loss caused by the reverse recovery of FWD is not included in  $E_{\text{on}}$ .

## Built-in SiC Diode Characteristics ( $T_j=25^\circ\text{C}$ )

Parameter	Symbol	Test Conditions	Typ.	Unit
Inverse Diode Forward Voltage	$V_{\text{SD}}$	$V_{\text{GS}}=-5\text{V}, I_{\text{SD}}=1.25\text{A}$	4.5	V
Reverse Recovery Time	$t_{\text{rr}}$	$V_{\text{GS}}=0\text{V},$ $I_{\text{SD}}=5\text{A}, V_{\text{DS}}=400\text{V},$ $di/dt=300\text{A}/\mu\text{s}$	50	ns
Reverse Recovery Charge	$Q_{\text{rr}}$		35	nC
Peak Reverse Recovery Current	$I_{\text{rrm}}$		1.8	A

## Gate Charge Characteristics ( $T_j=25^\circ\text{C}$ )

Parameter	Symbol	Test Conditions	Value	Unit
Gate to Source Charge	$Q_{GS}$	$V_{DS}=400\text{V}$ , $V_{GS}=-5/+20\text{V}$ , $I_D=5\text{A}$	10	nC
Gate to Drain Charge	$Q_{GD}$		19	
Total Gate Charge	$Q_G$		43	
Gate plateau voltage	$V_{pl}$		8.7	V

## Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta,JC}$	1.4	K/W
Thermal Resistance, Junction to Ambient	$R_{\theta,JA}$	TBD	

## Typical Device Performance

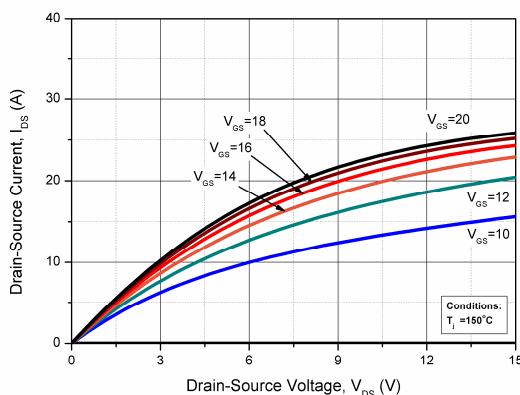
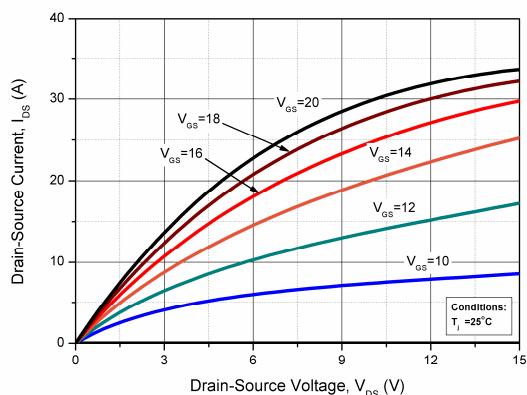


Fig. 1 Forward Output Characteristics at  
 $T_j = 25^\circ\text{C}$

Fig. 2 Forward Output Characteristics at  
 $T_j = 150^\circ\text{C}$

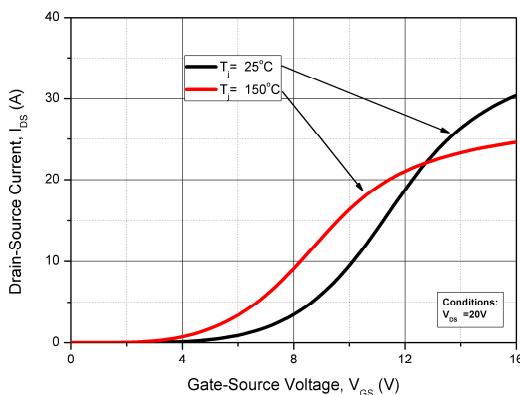
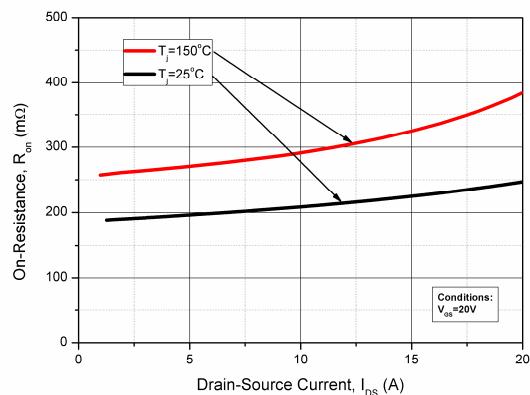
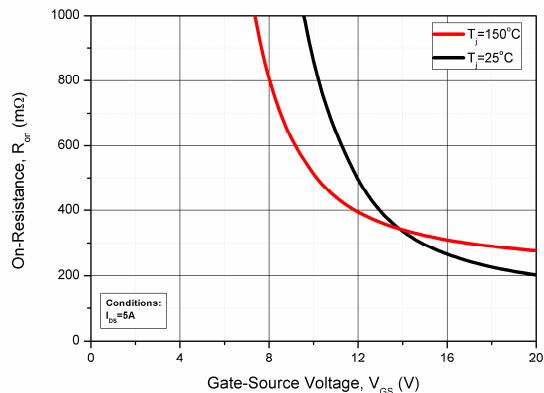


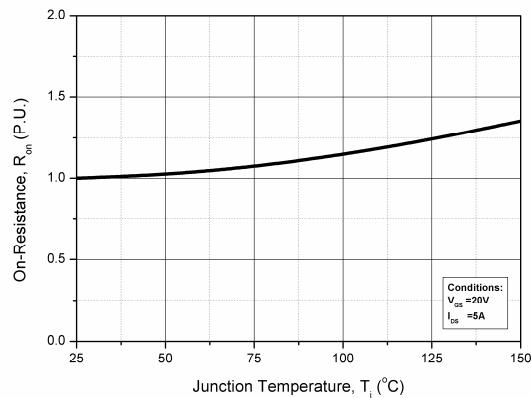
Fig. 3 On-Resistance vs. Drain Current for  
Various  $T_j$

Fig. 4 Transfer Characteristics for Various  $T_j$

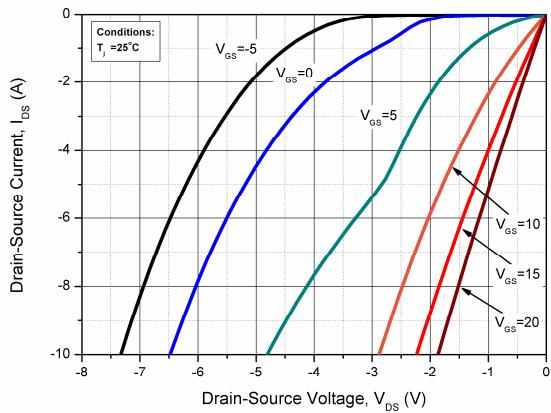
## Typical Device Performance



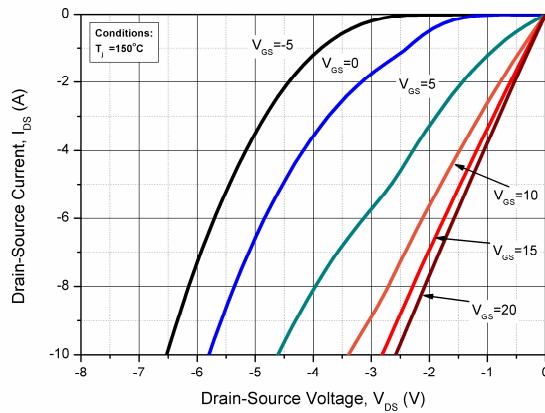
**Fig. 5 On-Resistance vs. Gate Voltage for Various  $T_j$**



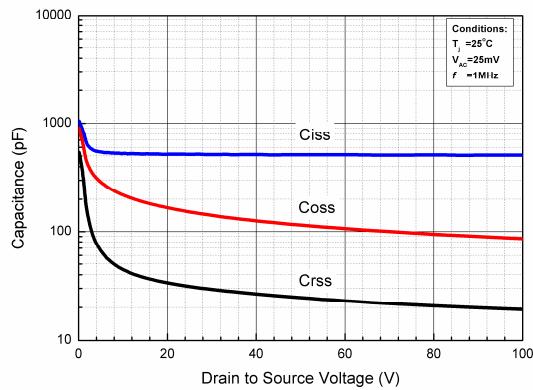
**Fig. 6 Normalized On-Resistance vs. Temperature**



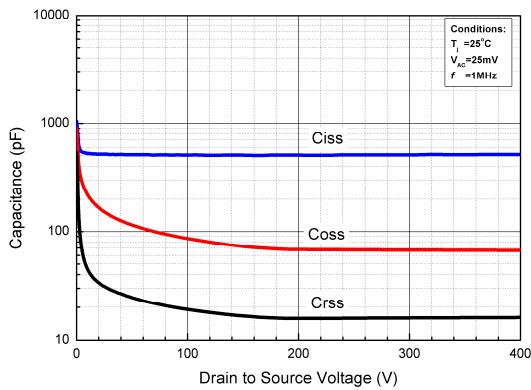
**Fig. 7 Reverse Output Characteristics at  $T_j = 25^\circ\text{C}$**



**Fig. 8 Reverse Output Characteristics at  $T_j = 150^\circ\text{C}$**



**Fig. 9 Capacitances vs. Drain to Source Voltage (0 - 100V)**



**Fig. 10 Capacitances vs. Drain to Source Voltage (0 - 400V)**

## Typical Device Performance

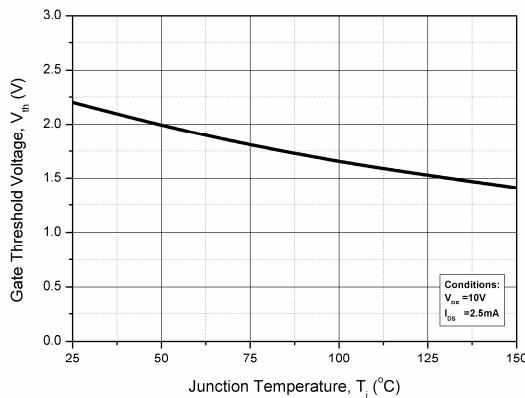


Fig. 11 Threshold Voltage vs. Temperature

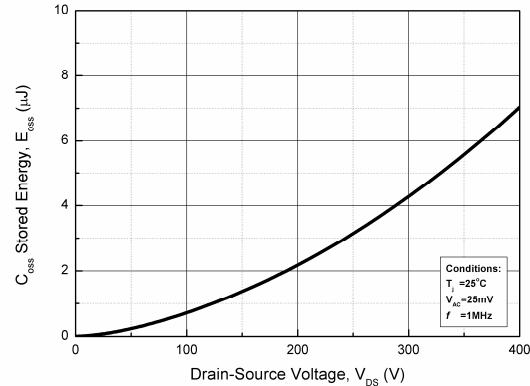


Fig. 12 Output Capacitor Stored Energy\*

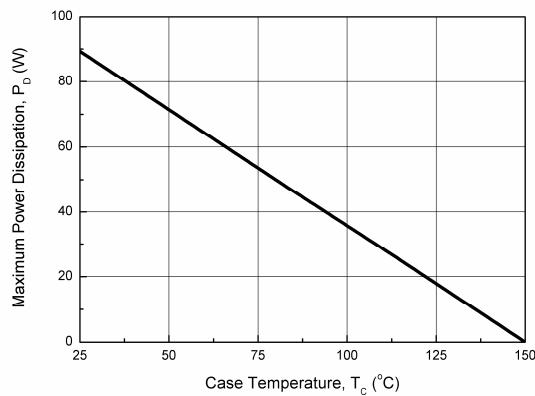


Fig. 13 Maximum Power Dissipation Derating vs. Case Temperature

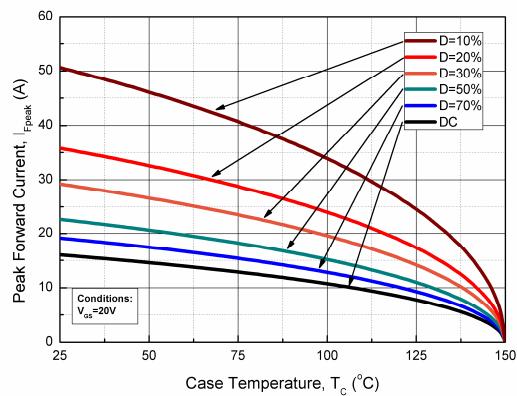


Fig. 14 Drain Current Derating vs. Case Temperature

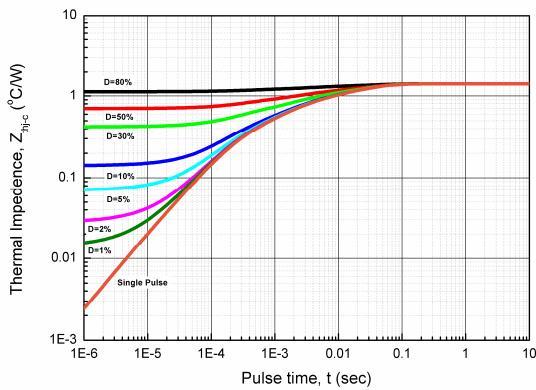


Fig. 15 Transient Junction to Case Thermal Impedance

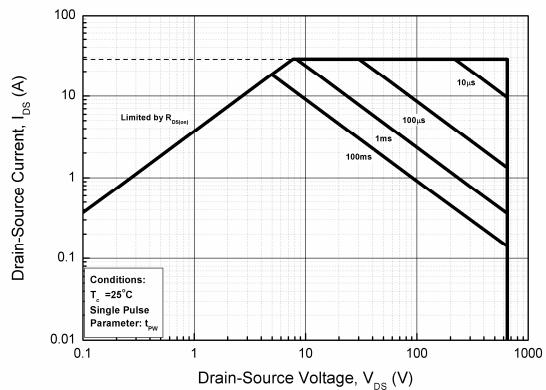


Fig. 16 Safe Operating Area

## Typical Device Performance

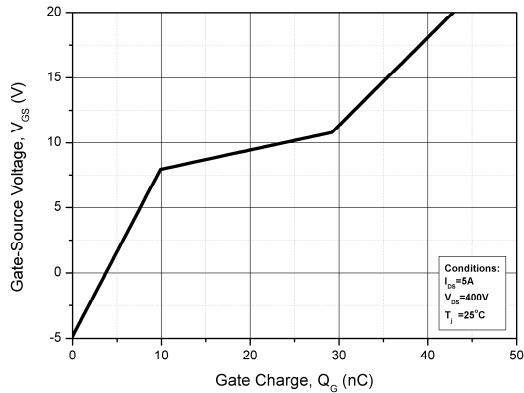


Fig. 17 Gate Charge Characteristics

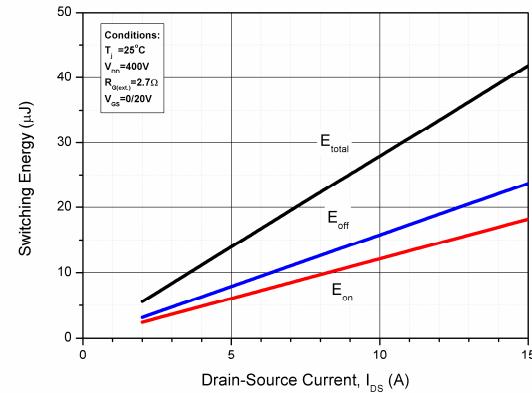


Fig. 18 Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD}=400V$ )\*

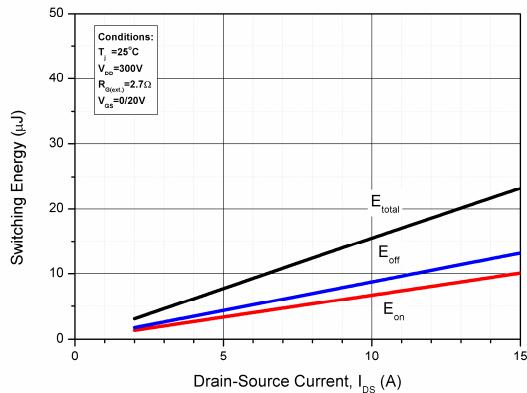


Fig. 19 Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD}=300V$ )\*

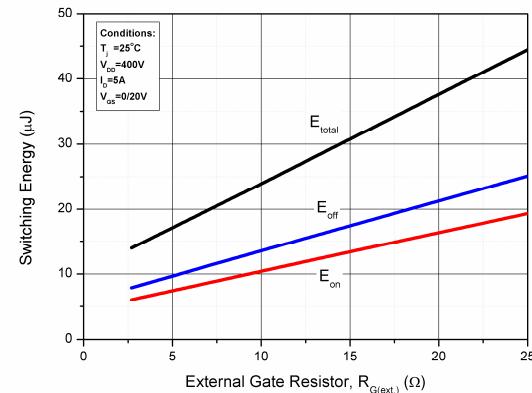
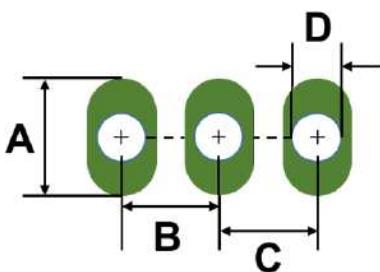


Fig. 20 Clamped Inductive Switching Energy vs. External Gate Resistor ( $R_{G(ext.)}$ )\*

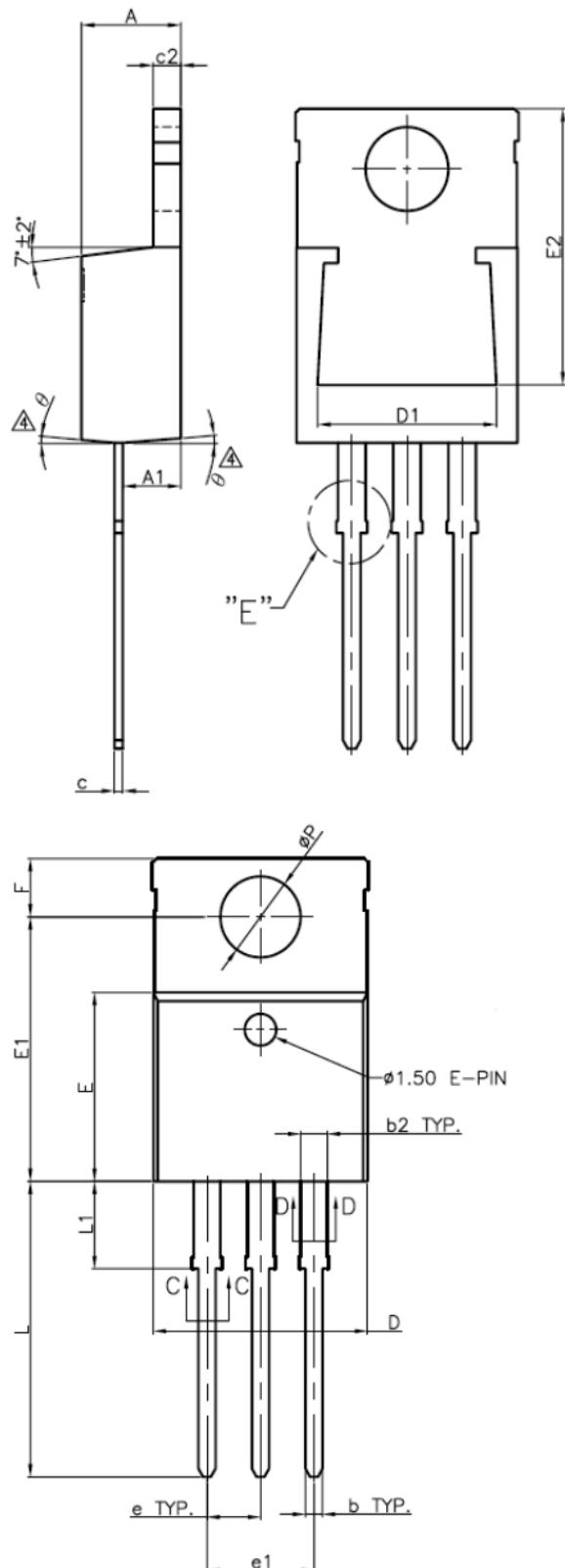
\*Base on the results of calculation, note that the energy loss caused by the reverse recovery of FWD is not included in  $E_{on}$ .

## Recommended Solder Pad Layout (TO-220-3L)

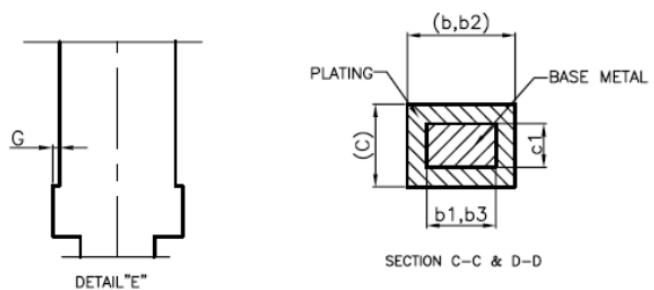


Mechanical Parameters			
Parameter	Symbol	Typical	Unit
Length	A	3.048	mm
	B	2.540	
	C	2.540	
	D	1.270	

## Mechanical Parameters



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	4.470	---	4.670	0.176	---	0.184
A1	2.520	---	2.820	0.099	---	0.111
b	0.711	0.813	0.910	0.028	0.032	0.036
b1	0.711	---	0.914	0.028	---	0.036
b2	1.170	1.270	1.370	0.046	0.050	0.054
b3	1.168	---	1.372	0.046	---	0.054
c	0.279	0.381	0.483	0.011	0.015	0.019
c1	0.279	---	0.432	0.011	---	0.017
c2	1.168	1.270	1.370	0.046	0.050	0.054
D	10.010	---	10.310	0.394	---	0.406
D1	7.595	---	8.230	0.299	---	0.324
E	8.763	8.890	9.017	0.345	0.350	0.355
E1	12.294	12.446	12.586	0.484	0.490	0.496
E2	11.913	---	12.548	0.469	---	0.494
e	---	2.540	---	---	0.100	---
e1	4.980	---	5.180	0.196	---	0.204
F	2.642	2.743	2.946	0.104	0.108	0.116
G	0.000	---	0.152	0.000	---	0.006
L	13.700	---	14.100	0.539	---	0.555
L1	3.980	4.107	4.230	0.157	0.162	0.167
φP	3.770	---	3.890	0.148	---	0.153
θ	1°	---	5°	1°	---	5°



NOTES:  
1. All dimensions are in mm [inch].  
2. Tolerance:  $\pm 0.004$  inch.

\*The information provided herein is subject to change without notice.