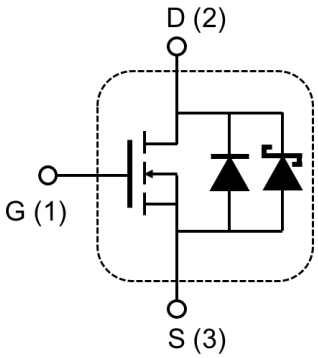
H1J120F060

Silicon Carbide Power MOSFET

N-CHANNEL ENHANCEMENT MODE
With JMOS Technology

TO-247-3L

Inner Circuit



Product Summary

V_{DS}	1200V
$I_{D(@25°C)}$	41A
$R_{DS(on)}$	60mΩ

RoHS COMPLIANT | Halogen free | AEC-Q101 QUALIFIED

Features

- Low On-Resistance
- Low Capacitance
- Avalanche Ruggedness
- Halogen Free, RoHS Compliant

Benefits

- Higher System Efficiency
- Parallel Device Convenience
- High Temperature Application
- High Frequency Operation

Applications

- SMPS / UPS / PFC
- EV Charging station & Motor Drives
- Power Inverters & DC/DC Converters
- Solar/ Wind Renewable Energy

Maximum Ratings (T_C=25°C)

Parameter	Symbol	Test Conditions	Value	Unit
Drain – Source Voltage	$V_{DS, max}$	V_{GS}=0V, I_{DS}=100μA	1200	V
Continuous Drain Current	I_D	V_{GS}=20V, T_C=25°C	41	A
		V_{GS}=20V, T_C=110°C	25	
Pulse Drain Current	$I_{D, pulse}$	t_{PW} limitation per Fig.16	138	
Avalanche energy, Single Pulse	E_{AS}	V_{DD}=100V, I_D=10A	1250	mJ
Power Dissipation	P_D	T_C=25°C	208	W
Recommend Gate Source Voltage	$V_{GS, op}$		-5/+20	V
Maximum Gate Source Voltage	$V_{GS, max}$		-10/+25	
Junction & Storage Temperature	T_j , T_{stg}		-55/+150	°C
Soldering Temperature	T_L		260	

Electrical Characteristics (T_j=25°C)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_{DS}=100μA	1200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=10V, I_{DS}=10mA		2.4		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=1200V, V_{GS}=0V		<1	50	μA
		V_{DS}=1200V, V_{GS}=0V T_j=150°C		5	200	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=20V, V_{DS}=0V			250	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=20V, I_{DS}=20A		60	80	mΩ
		V_{GS}=20V, I_{DS}=20A, T_j=150°C		95		
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=800V *f* =1MHz, V_{AC}=25mV		1900		pF
Output Capacitance	C_{oss}			102		
Reverse Transfer Capacitance	C_{rss}			23		
Effective Output Capacitance, Energy Related	$C_{o(er)}$	V_{GS}=0V, V_{DS}=0 to 800V		123		
Effective Output Capacitance, Time Related	$C_{o(tr)}$	I_D=const., V_{GS}=0V, V_{DS}=0 to 800V		164		
Turn On Delay Time	$t_{d(on)}$	V_{DS}=800V, V_{GS}=-4/+20V, I_D=20A, R_L=40Ω, $R_{G(ext)}$= 2.7 Ω		25		ns
Rise Time	t_r			24		
Turn Off Delay Time	$t_{d(off)}$			20		
Fall Time	t_f			9		
C_{oss} Stored Energy	E_{oss}	V_{GS}=0V, V_{DS}=800V *f* =1MHz, V_{AC}=25mV		52*		μJ
Turn-on Switching Energy	E_{on}	V_{DS}=800V, V_{GS}=0/20V, I_D=20A, $R_{G(ext)}$= 2.7 Ω		114*		
Turn-off Switching Energy	E_{off}			155*		
Internal Gate Resistance	$R_{G(int.)}$	*f* =1MHz, V_{AC}=25mV		4		Ω

*Base on the results of calculation, note that the energy loss caused by the reverse recovery of FWD is not included in E_{on}.

Built-in SiC Diode Characteristics (T_j=25°C)

Parameter	Symbol	Test Conditions	Typ.	Unit
Inverse Diode Forward Voltage	V_{SD}	V_{GS}=-5V, I_{SD}=10A	3.0	V
Continuous Diode Forward Current	I_S	V_{GS}=-5V, T_C=25°C	27	A
Reverse Recovery Time	t_{rr}	V_{GS}=0V, I_{SD}=20A, V_{DS}=400V, di/dt=300A/μs	59	ns
Reverse Recovery Charge	Q_{rr}		84	nC
Peak Reverse Recovery Current	I_{rrm}		2.98	A

Gate Charge Characteristics (T_j=25°C)

Parameter	Symbol	Test Conditions	Value	Unit
Gate to Source Charge	Q_{GS}	V_{DS}=800V, V_{GS}=-5/+20V, I_D=20A	31	nC
Gate to Drain Charge	Q_{GD}		56	
Total Gate Charge	Q_G		128	
Gate plateau voltage	V_{pl}		7.7	V

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta,JC}$	0.6	K/W
Thermal Resistance, Junction to Ambient	$R_{\theta,JA}$	TBD	

Typical Device Performance

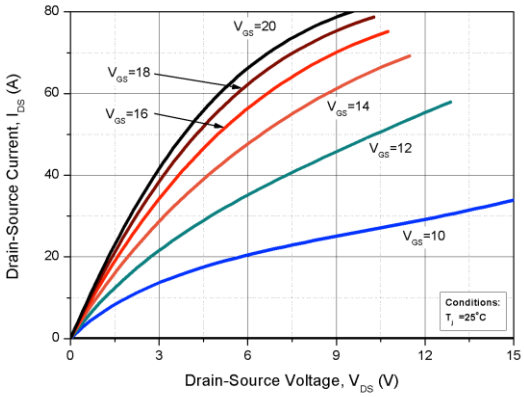


Fig. 1 Forward Output Characteristics at T_j = 25°C

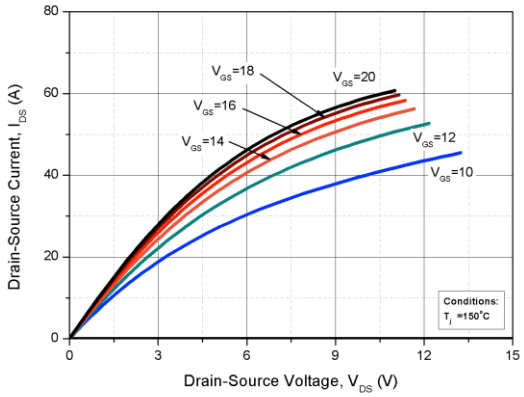


Fig. 2 Forward Output Characteristics at T_j = 150°C

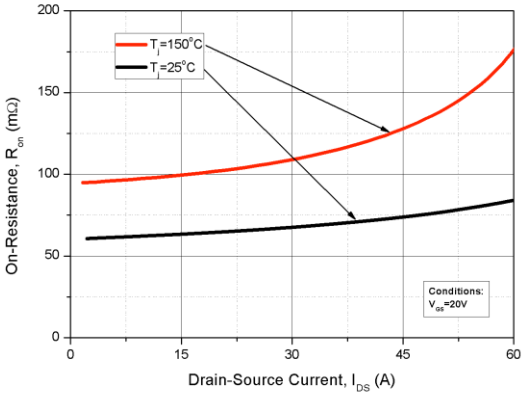


Fig. 3 On-Resistance vs. Drain Current for Various T_j

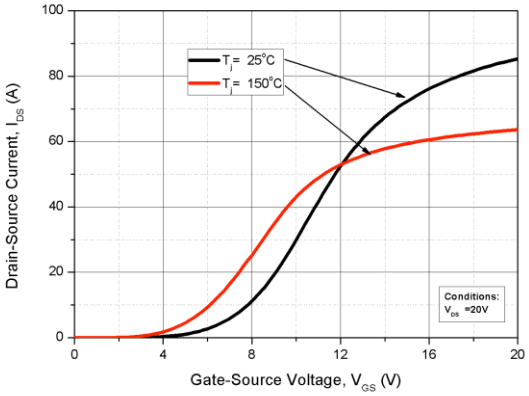


Fig. 4 Transfer Characteristics for Various T_j

Typical Device Performance

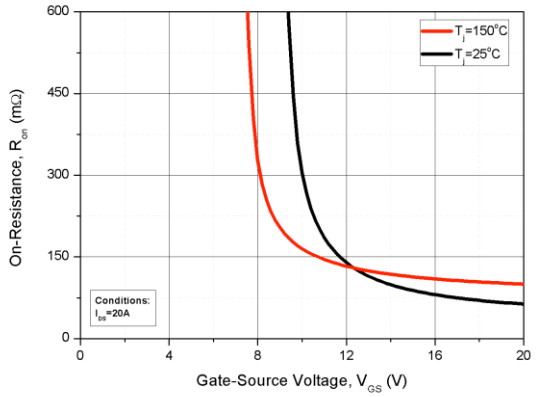


Fig. 5 On-Resistance vs. Gate Voltage for Various T_j

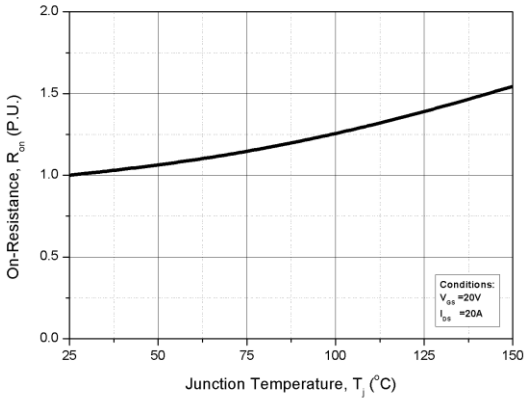


Fig. 6 Normalized On-Resistance vs. Temperature

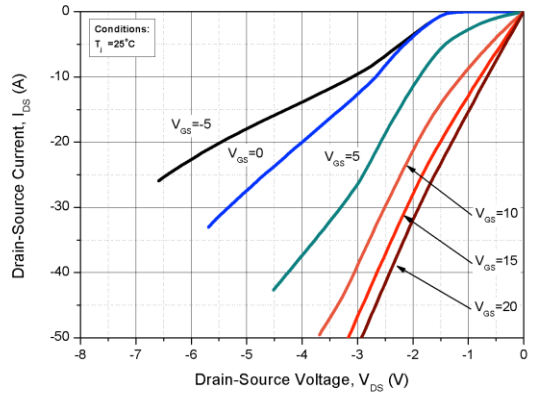


Fig. 7 Reverse Output Characteristics at T_j = 25°C

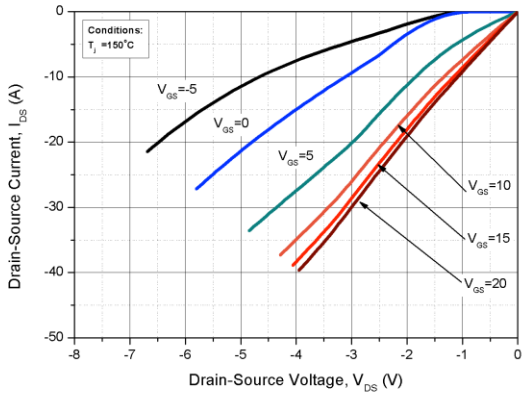


Fig. 8 Reverse Output Characteristics at T_j = 150°C

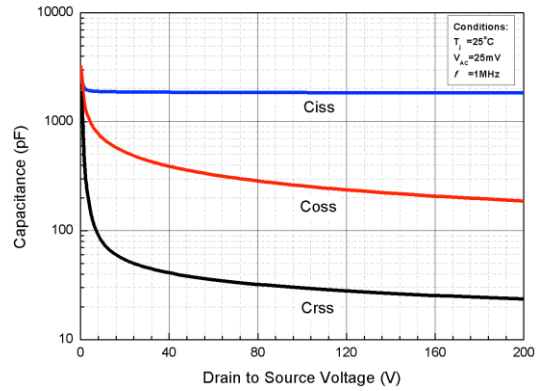


Fig. 9 Capacitances vs. Drain to Source Voltage (0 - 200V)

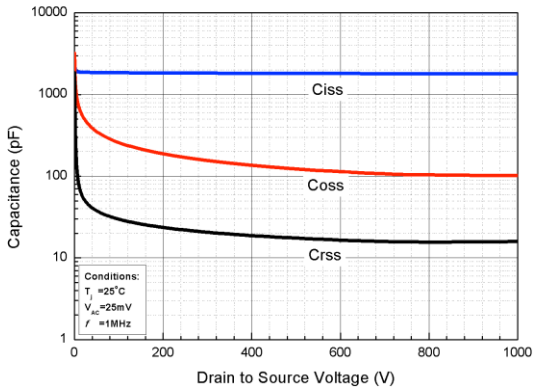


Fig. 10 Capacitances vs. Drain to Source Voltage (0 - 1000V)

Typical Device Performance

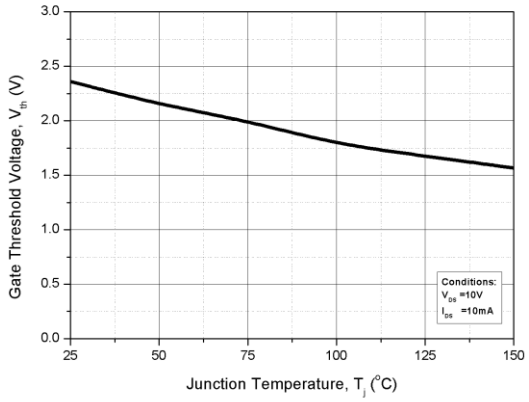


Fig. 11 Threshold Voltage vs. Temperature

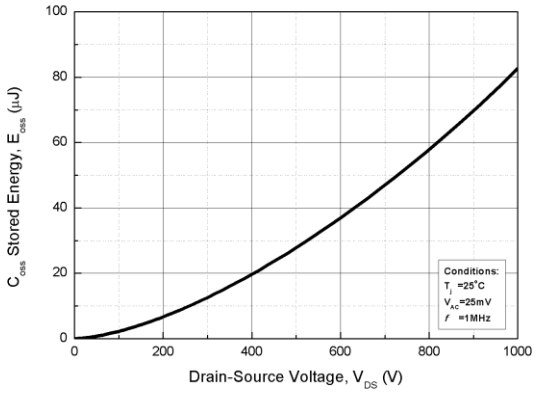


Fig. 12 Output Capacitor Stored Energy*

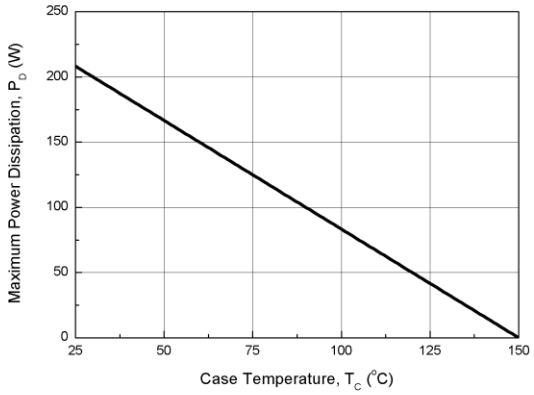


Fig. 13 Maximum Power Dissipation Derating vs. Case Temperature

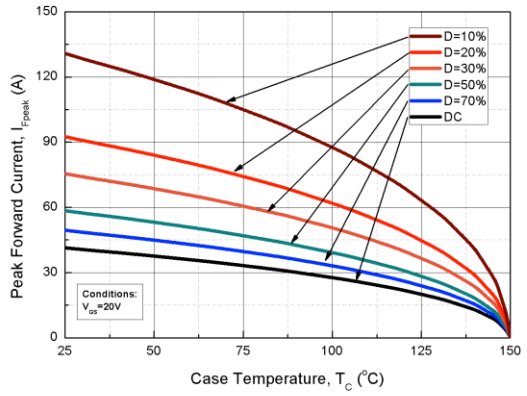


Fig. 14 Drain Current Derating vs. Case Temperature

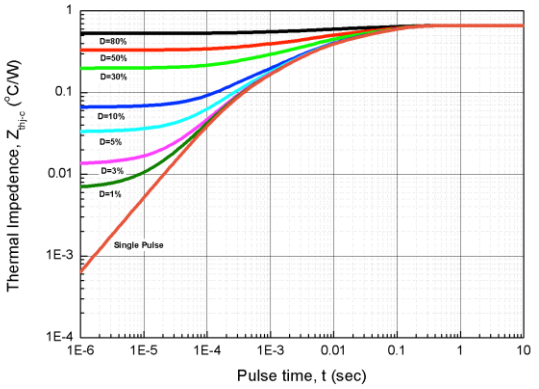


Fig. 15 Transient Junction to Case Thermal Impedance

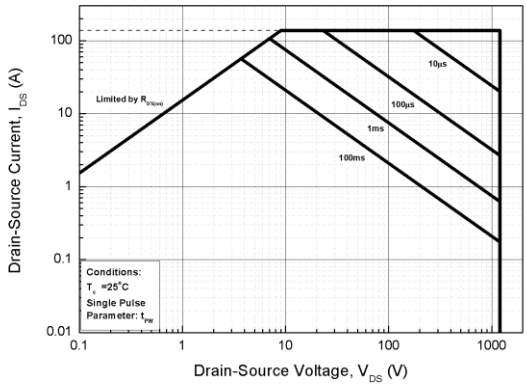


Fig. 16 Safe Operating Area

Typical Device Performance

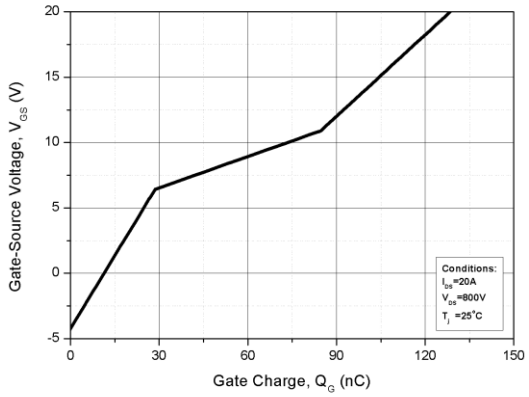


Fig. 17 Gate Charge Characteristics

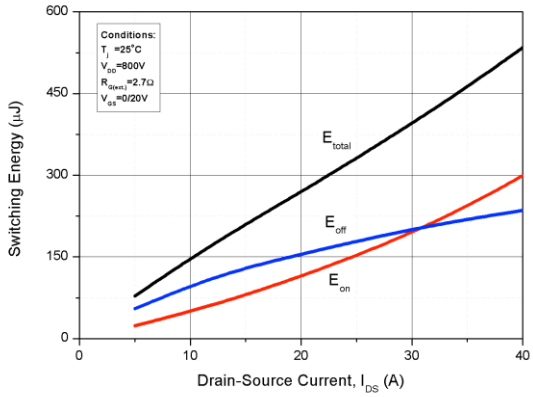


Fig. 18 Clamped Inductive Switching Energy vs. Drain Current (V_{DD}=800V)*

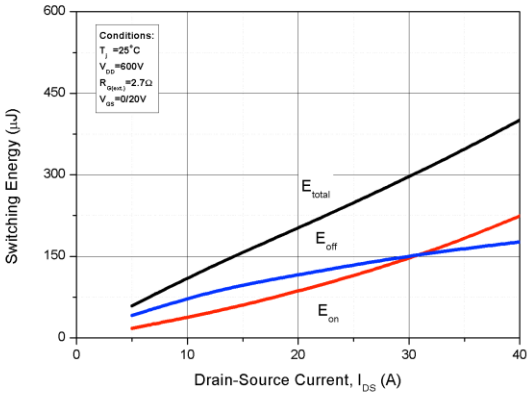


Fig. 19 Clamped Inductive Switching Energy vs. Drain Current (V_{DD}=600V)*

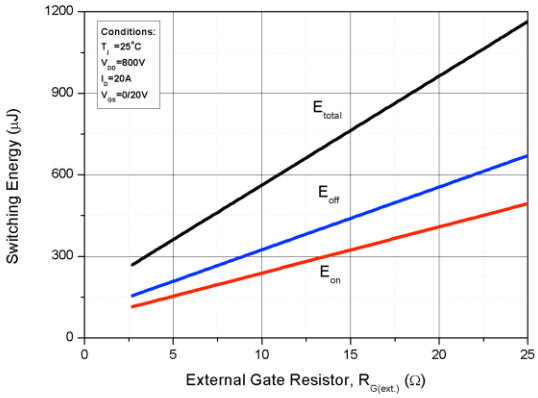
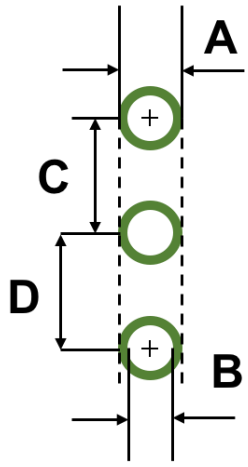


Fig. 20 Clamped Inductive Switching Energy vs. External Gate Resistor ($R_{G(ext.)}$)*

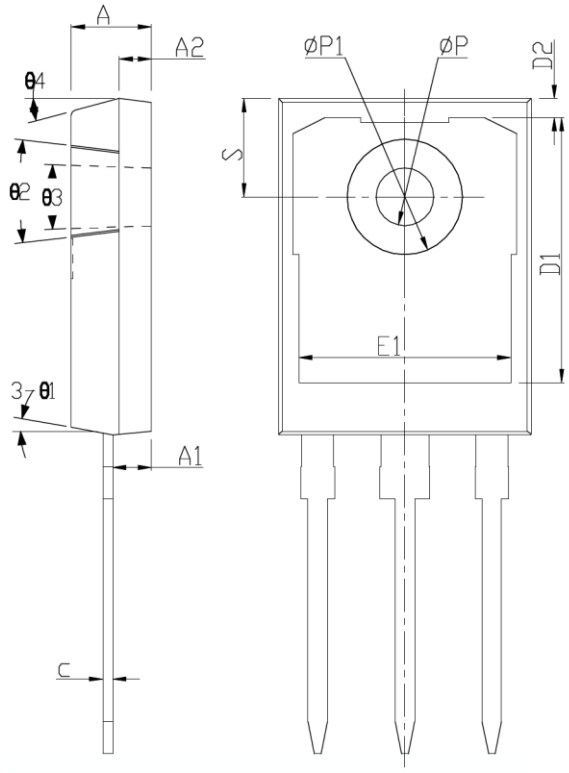
*Base on the results of calculation, note that the energy loss caused by the reverse recovery of FWD is not included in E_{on}.

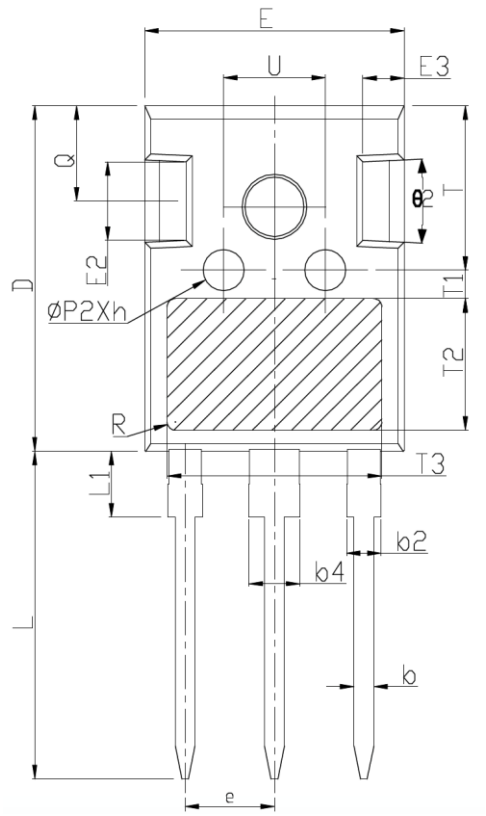
Recommended Solder Pad Layout (TO-247-3L)

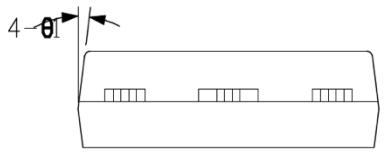


Mechanical Parameters			
Parameter	Symbol	Typical	Unit
Length	A	3.048	mm
	B	2.032	
	C	5.436	
	D	5.436	

Mechanical Parameters







SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	4.75	5.00	5.25
A1	2.16	2.41	2.66
A2	1.85	2.00	2.15
b	1.11	1.21	1.35
b2	1.90	2.01	2.25
b4	2.90	3.01	3.25
c	0.51	0.61	0.75
D	20.60	21.00	21.40
D1	16.15	16.55	16.95
D2	1.00	1.20	1.40
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.70	5.00	5.30
E3	2.25	2.50	2.75
e		5.44BSC	
h	0.00	0.10	0.25
L	19.52	19.92	20.32
L1	-	-	4.30
ΦP	3.35	3.60	3.85
ΦP1	-	-	7.30
ΦP2	2.25	2.50	2.75
Q	5.50	5.80	6.10
S		6.15BSC	
R		0.50REF	
T	9.70	-	10.30
T1		1.65REF	
T2		8.00REF	
T3		12.80REF	
U	5.90	-	6.50
θ1	4°	7°	10°
θ2	2°	5°	8°
θ3	1°	-	2°
θ4	10°	15°	20°

NOTES:
1.All dimensions are in mm.
2.Tolerance: ±0.05mm.

*The information provided herein is subject to change without notice.